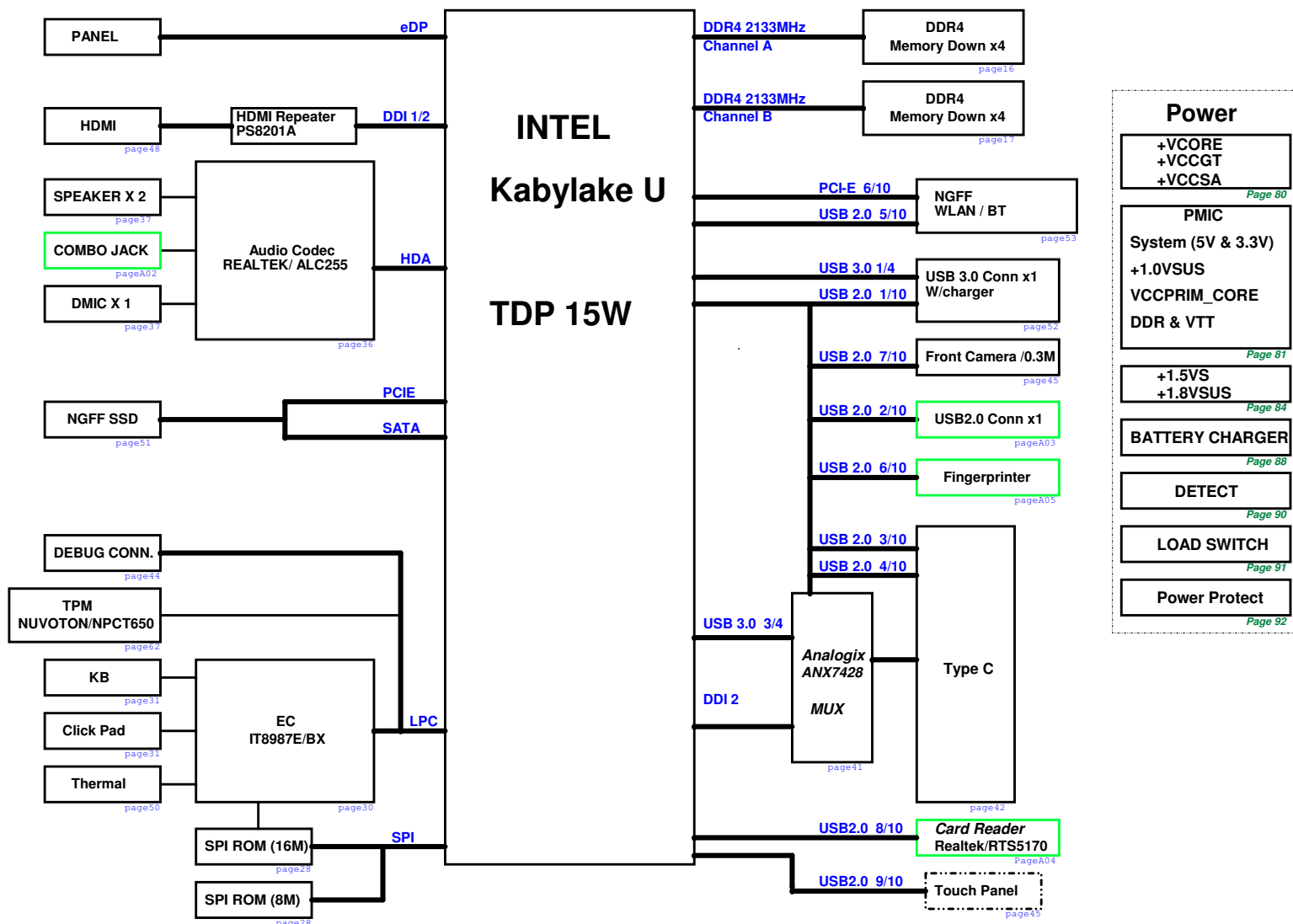


01. Block Diagram
 02. GPIO Setting
 03. CPU(1)_DDI/eDP
 04. CPU(2)_DDR4
 05. CPU(3)_+VCCCORE
 06. CPU(4)_+VCCGT
 07. CPU(5)_+VDDQ/IO/SA
 08. CPU(6)_CPU GND
 09. CPU(7)_CFG/RSVD
 15. DDR4(0)_Termination
 16. DDR4(1)_CH0
 17. DDR4(2)_CH1
 19. DDR4(4)_CA/DQ Voltage
 20. PCH(1)_SPI/LPC
 21. PCH(2)_ISH
 22. PCH(3)_HDA/SDIO
 23. PCH(4)_USB/PCIE/SATA
 24. PCH(5)_CLK/RTC
 25. PCH(6)_POWER MANAGEMENT
 26. PCH(7)_POWER
 28. PCH(9)_SPI/SMB
 30. EC_IT8587/FX
 31. EC_IT8587/FX_KB/TP/KBBL
 32. RST_Reset Circuit
 36. AUD_ALC255
 37. AUD(2)_SPK/DMIC
 41. USB_Type-C ANX7428
 42. USB Type-C Receptacle
 43. USB Type-C Dead Battery
 44. Debug CONN
 45. CRT(1)_eDP,CAMERA,TSN
 47. HDMI Repeater PS8201A
 48. HDMI OUT
 50. THERMAL / FAN
 51. NGFF PCIE*4/SATA SSD
 52. USB 3.0/Sleep Charge IC
 53. NGFF PCIE WLAN/BT
 56. LED
 57. Discharge
 60. DC_DC/BAT CONN
 62. TPM NPCT650
 64. IO Board
 65. ME_CONN / Skew Hole
 68. BYPASS EC SEQUENCE
 80. POWER_VCORE for U22
 81. POWER_SYSTEM
 82. POWER_+1.0VSUS
 83. POWER_DDR & VTT_UMA
 84. POWER_1.8VSUS
 85. POWER_1.5VS
 86. POWER_XXX
 87. POWER_XXX
 88. POWER_CHARGER
 89. POWER_AC_PD_WC Input
 90. POWER_DETECT
 91. POWER_LOAD SWITCH
 92. POWER_PROTECT
 93. POWER_SIGNAL
 94. POWER_FLOWCHART
 A02. AUD(2)_JACK
 A03. USB20
 A04. CB_RTSS170_GR

14" CARDB(X3) & M3RDA(M3) for Kabylake U Platform Block Diagram



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Discharge Circuit

Page 57

DC & BATT. Conn.

Page 60

Reset Circuit

Page 32

Skew Holes

Page 65

<Variant Name>

PEGATRON Title : Block Diagram
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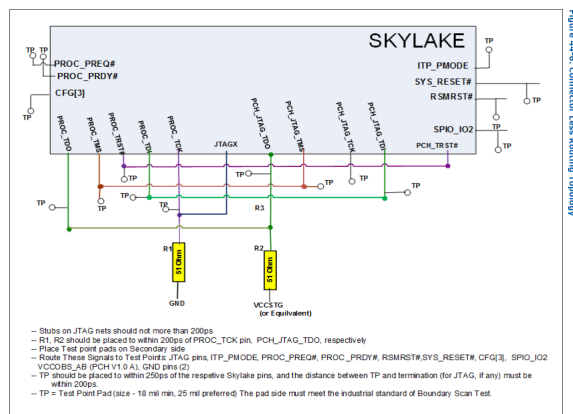
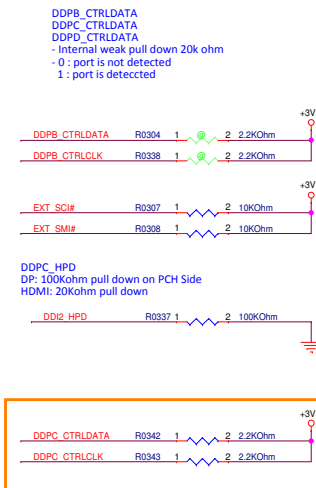
BG14HW3 Engineer: Andy Kao

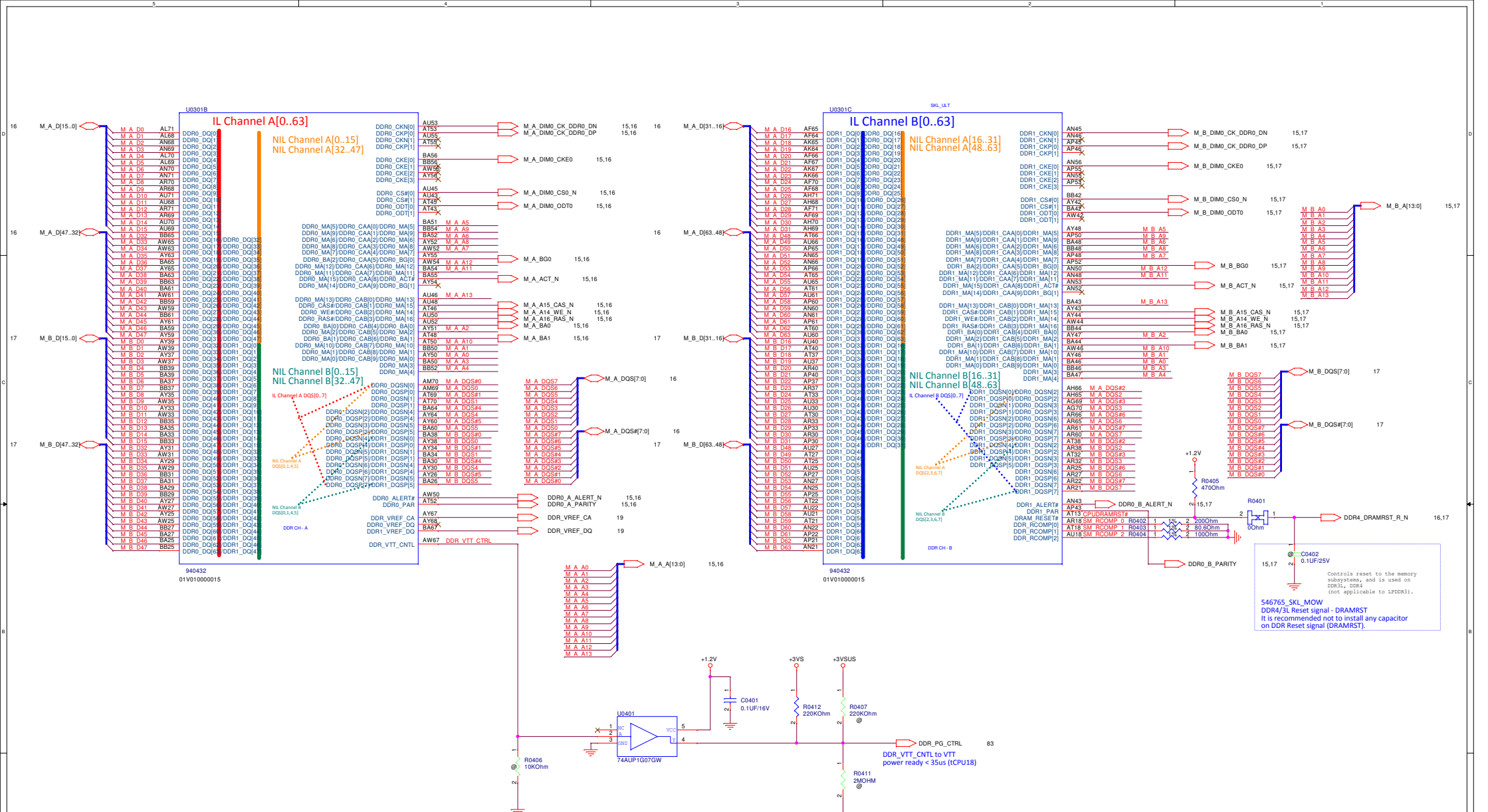
Size Project Name
 Custom X3

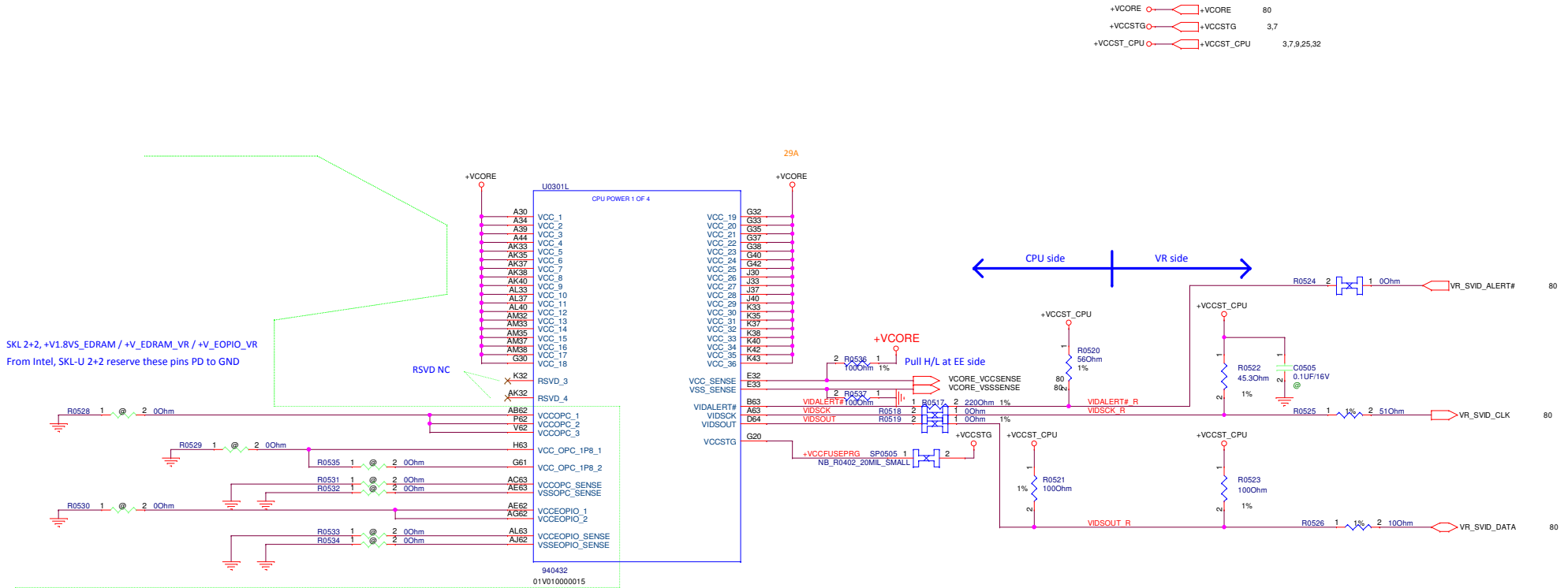
Date: Friday, October 21, 2016 Sheet 1 of 97

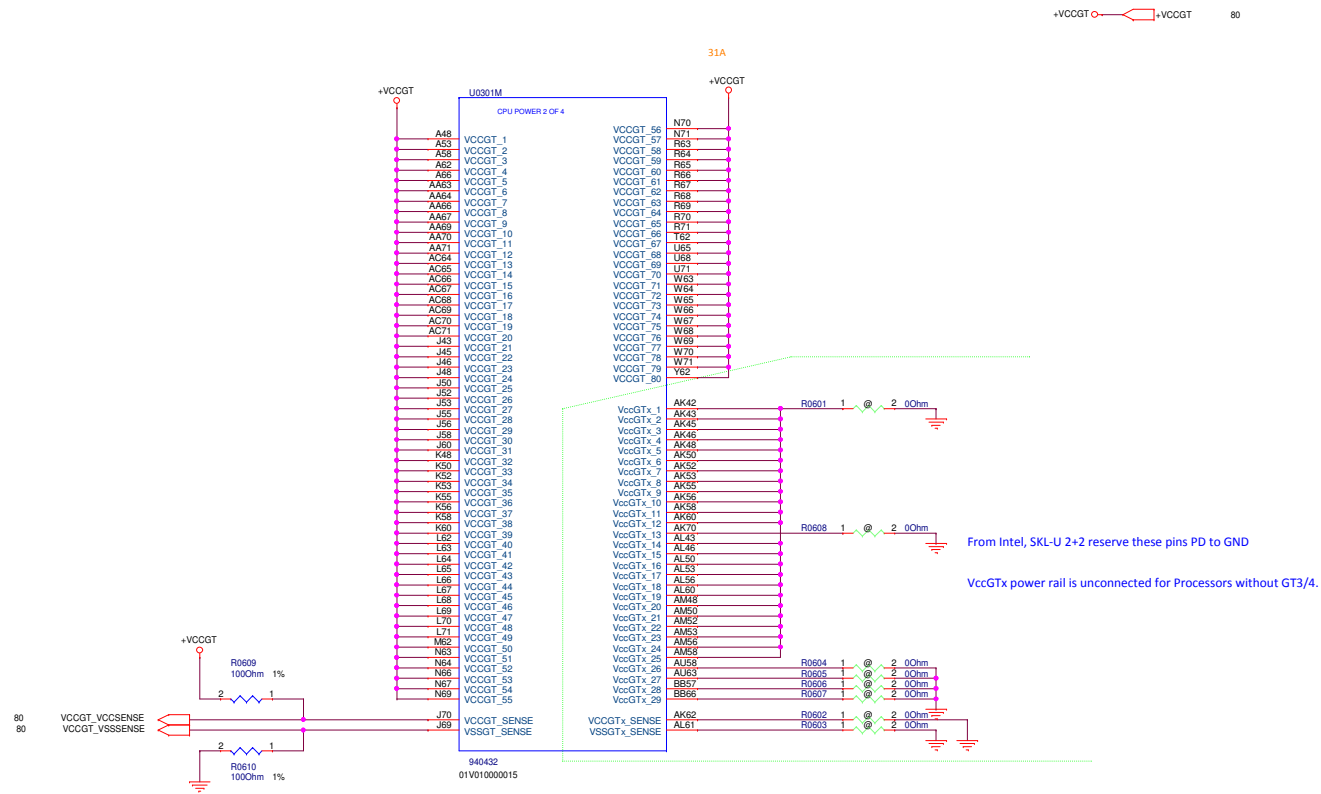
Rev 1.0

5			4			3			2			1														
EC GPIO			Use As			Signal Name			EC GPIO			Use As			Signal Name			EC GPIO			Use As			Signal Name		







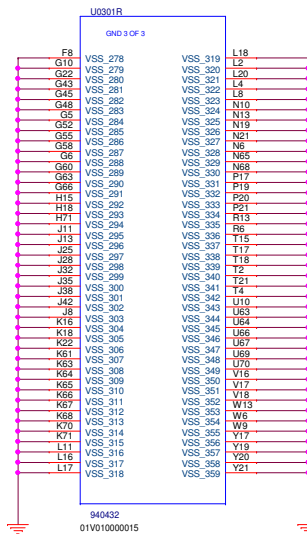
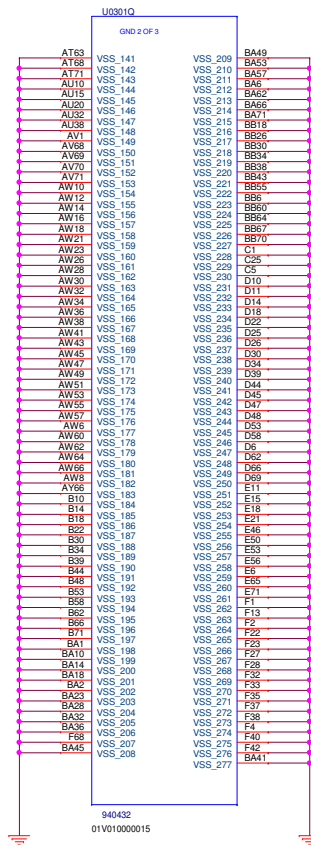
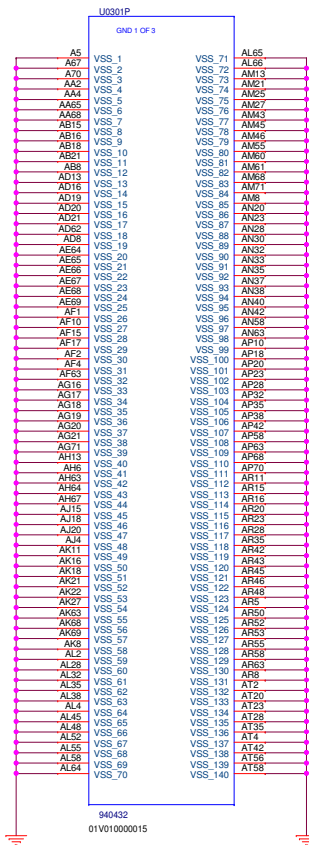


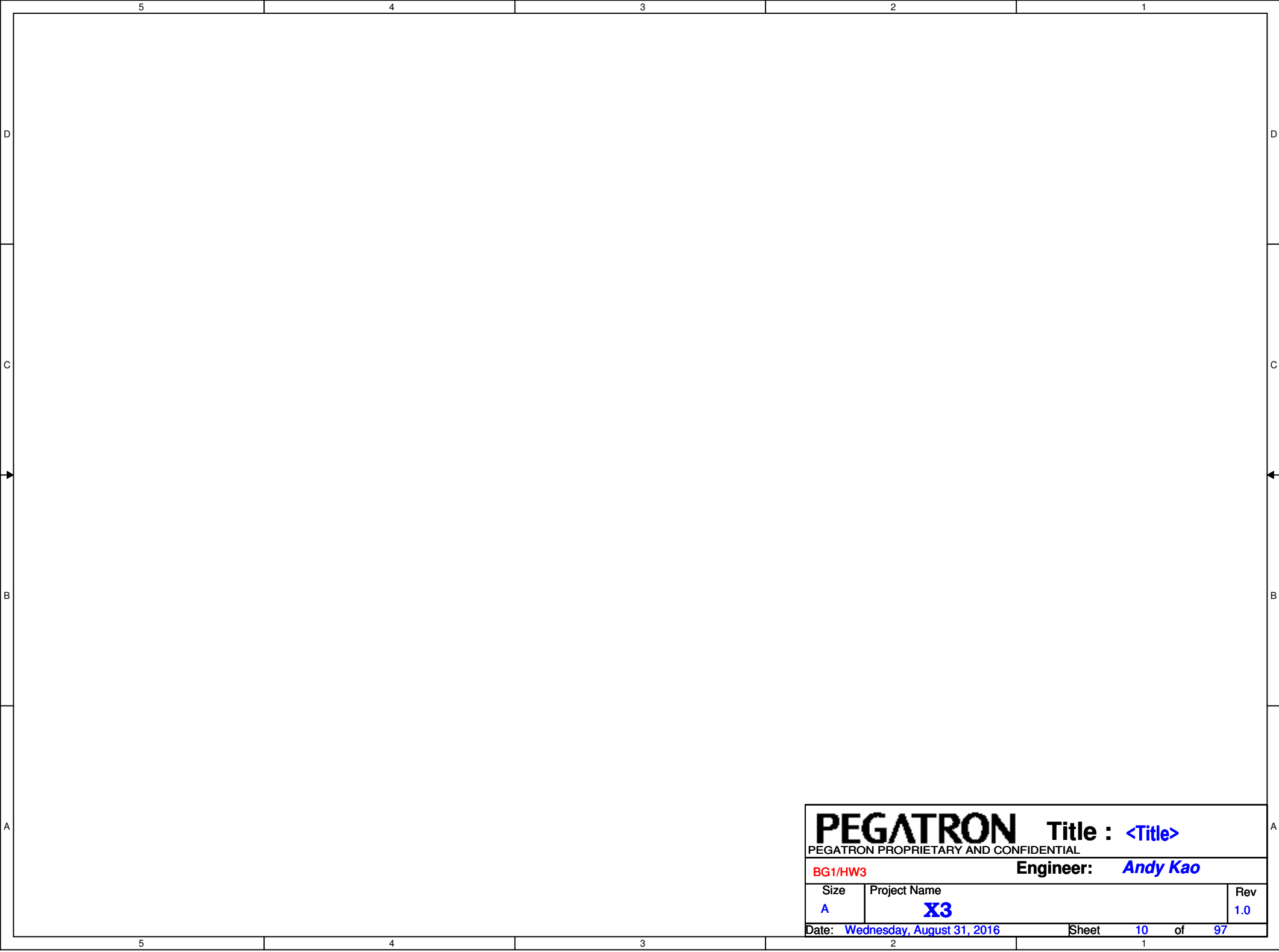
Power Rail Requirements – Volume Segment

The diagram illustrates the power rail requirements for the U0301N CPU, specifically for the VDDQ3 3 OF 4 and VDDQ3 4 OF 4 sections. The diagram shows the connection of various power rails (VDDQ, VCCST, VCCPL, VCCSA, VCCSFR, VCCIO) to the CPU pins. Key components include capacitors (C0701-C0716, C0717-C0720, C0711, C0712, C0713, C0714, C0715, C0716), resistors (R0701, R0702, R0703, R0710, R0711, R0713), and a diode (D0701). The diagram also shows the connection of the CPU pins to the power rails, with labels for the pin numbers and the power rail names. The diagram is divided into two main sections: the left section shows the power rail requirements for the VDDQ3 3 OF 4 section, and the right section shows the requirements for the VDDQ3 4 OF 4 section. The left section includes a table of power rail requirements for the VDDQ3 3 OF 4 section, and the right section includes a table of power rail requirements for the VDDQ3 4 OF 4 section. The tables list the power rail name, the pin number, and the required value (e.g., 100nF, 100Ohm, 100kOhm). The diagram also shows the connection of the CPU pins to the power rails, with labels for the pin numbers and the power rail names. The diagram is a detailed schematic showing the electrical connections between the CPU and the power rails, including capacitors, resistors, and diodes. It is a technical drawing used for engineering purposes.

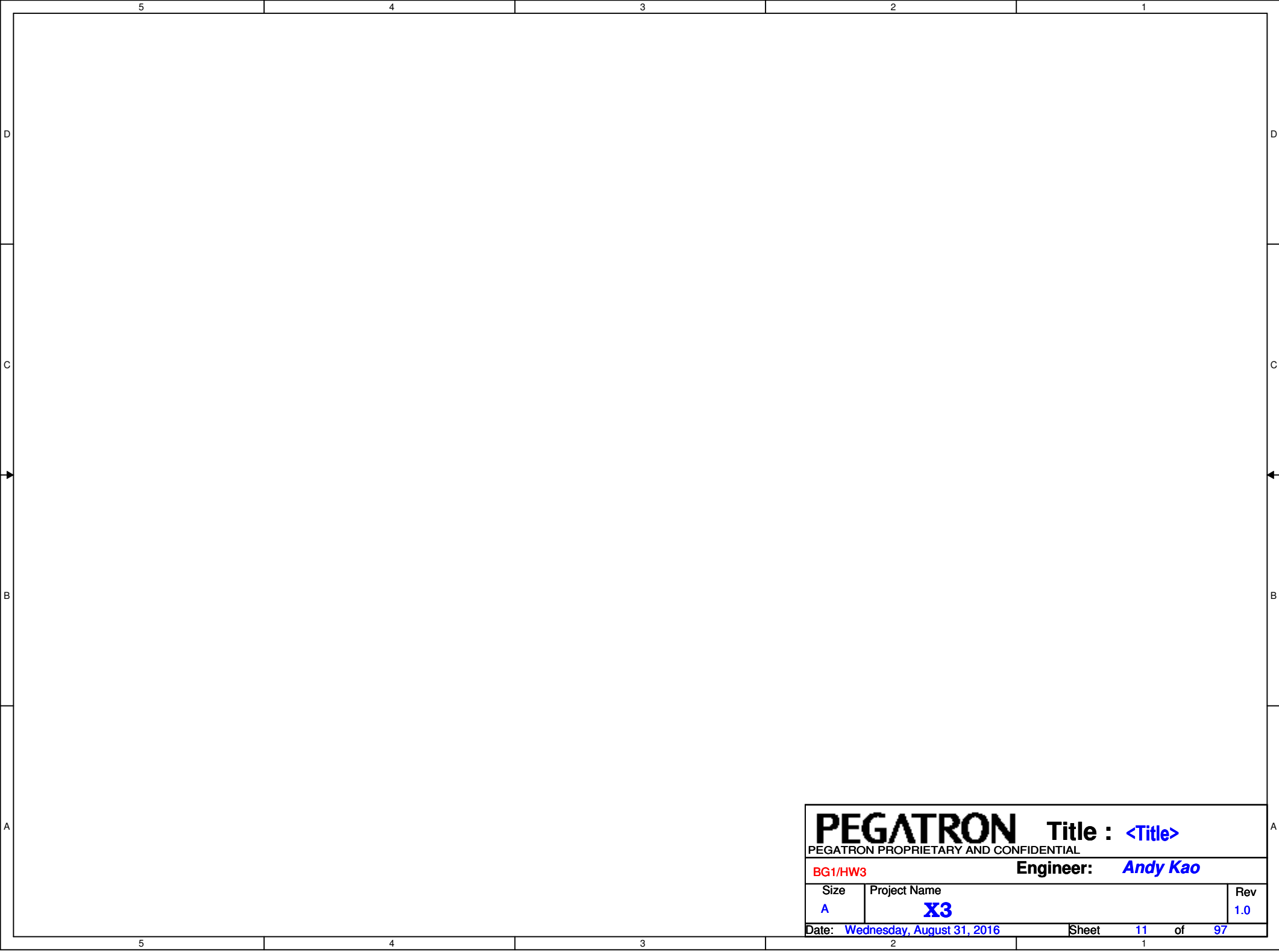
Load switch (LS)	LS ENABLE	Load/Rail name	I _{max} (A)
<= 65usec full load ready (Note 16)	SLP_S4#	VCC _{ST}	0.04
		VCC _{PLL} (VCC _{SFR})	0.12
<= 65usec full load ready	SLP_S3# AND SLP_S0#	VccIO	3.0
		VCC _{STG}	0.04

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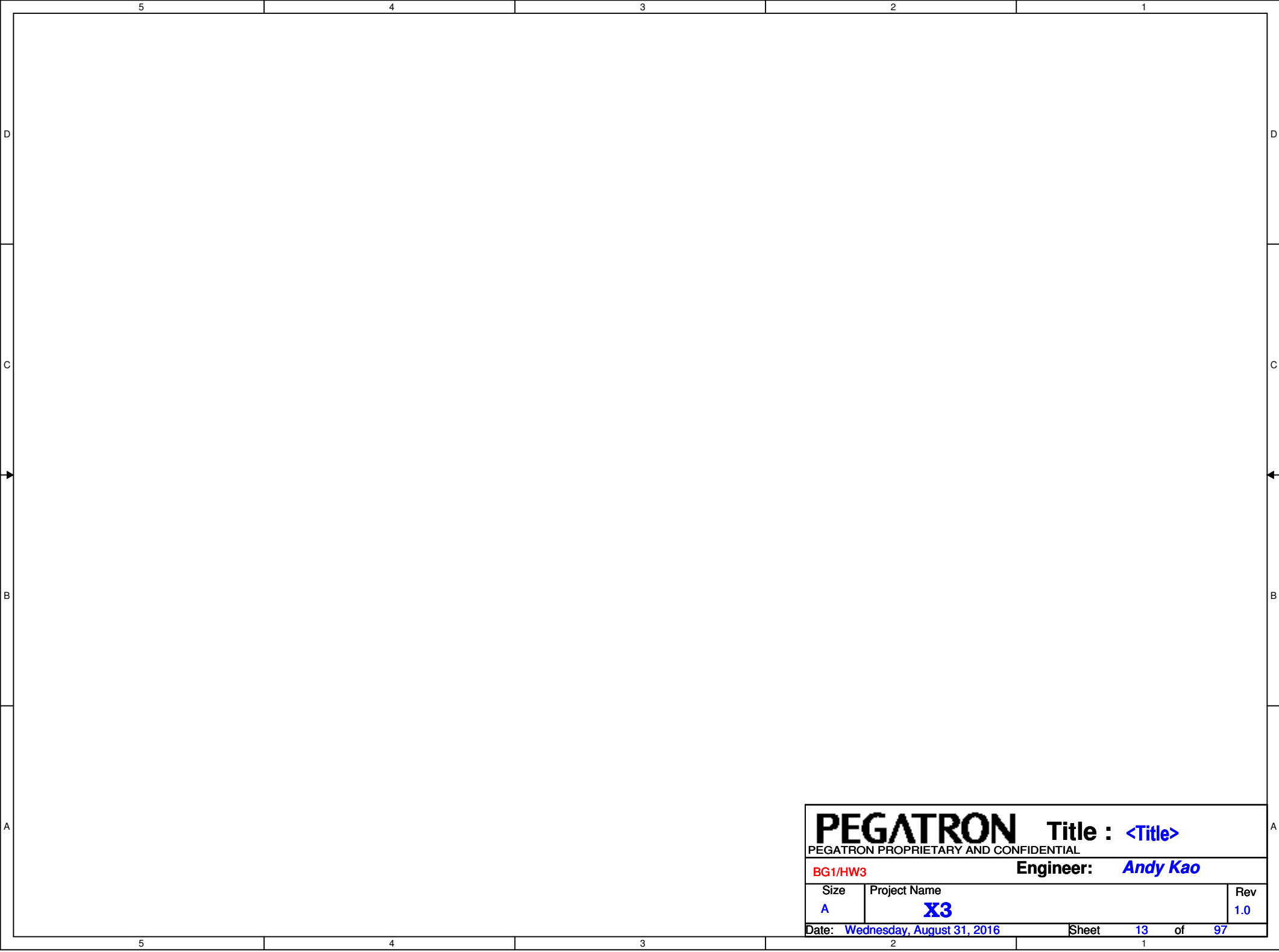




PEGATRON		Title : <Title>	
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BG1/HW3		Engineer: <i>Andy Kao</i>	
Size <i>A</i>	Project Name X3		Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>10</i> of <i>97</i>	



PEGATRON		Title : <Title>	
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BG1/HW3		Engineer: <i>Andy Kao</i>	
Size A	Project Name X3		Rev 1.0
Date: Wednesday, August 31, 2016		Sheet 11 of 97	



PEGATRON

Title : <Title>

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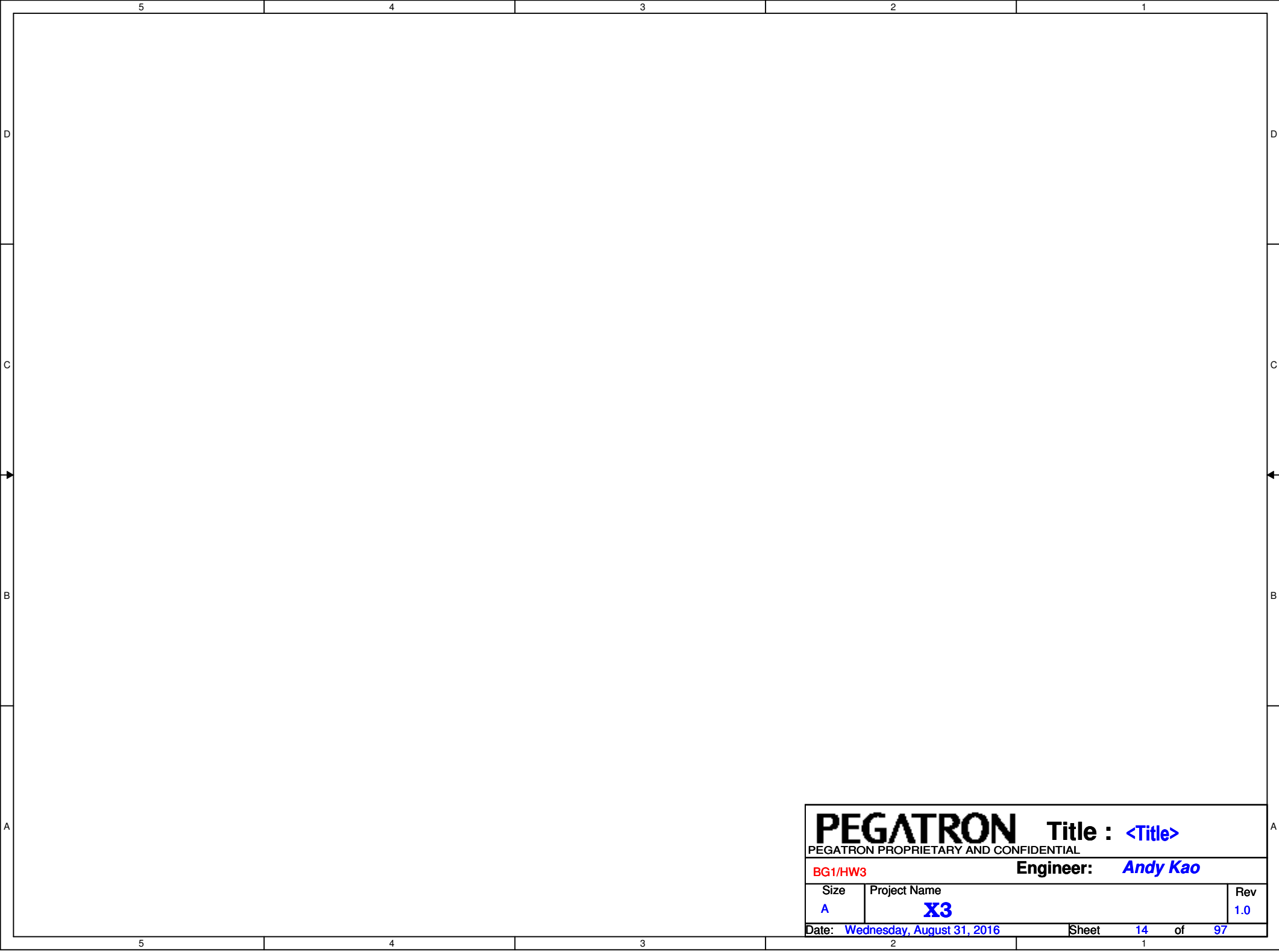
BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0



Date: Wednesday, August 31, 2016

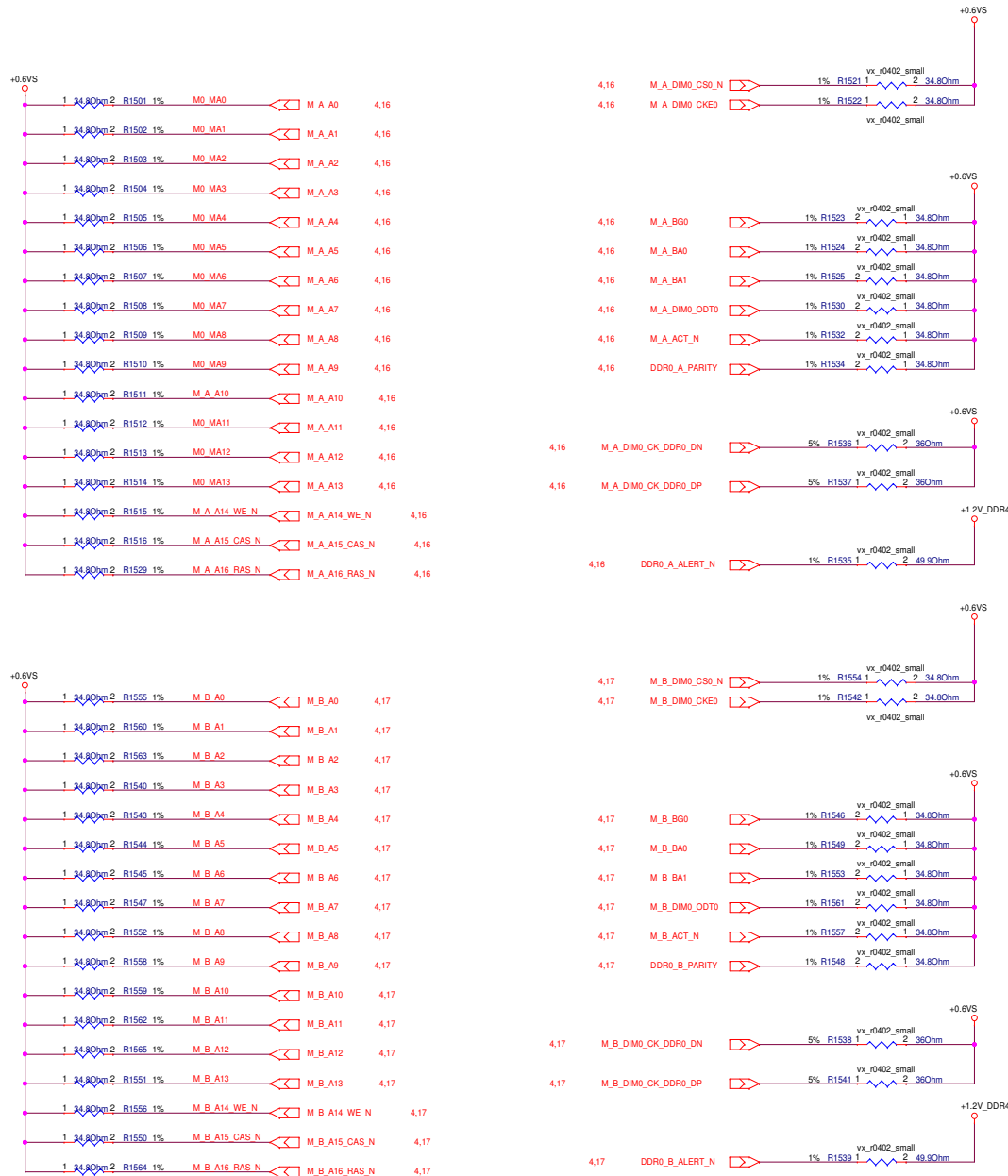
Sheet 13 of 97



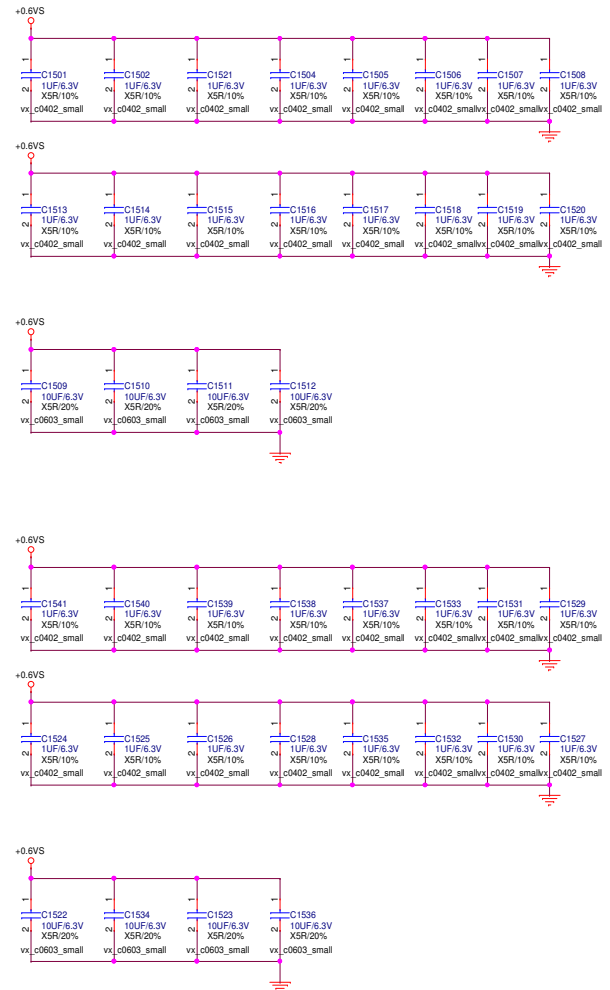
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size <i>A</i>	Project Name X3		Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>14</i> of <i>97</i>	

DDR4(0)_Termination

+0.6VS  +0.6VS 57,83
+1.2V_DDR4  +1.2V_DDR4 4,7,16,17,19,57,83

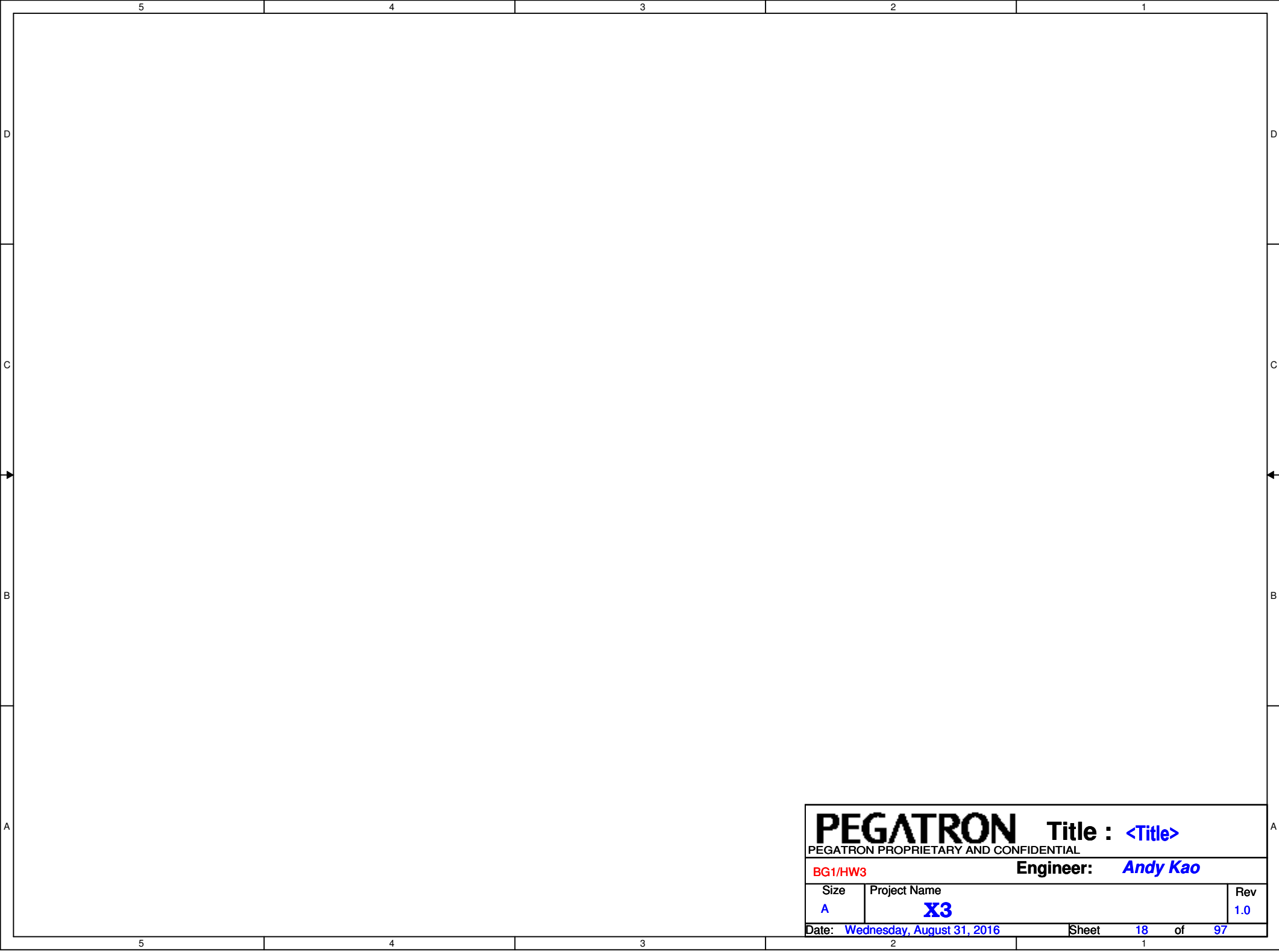


Average placed close to +VDDQ_VTT power plane





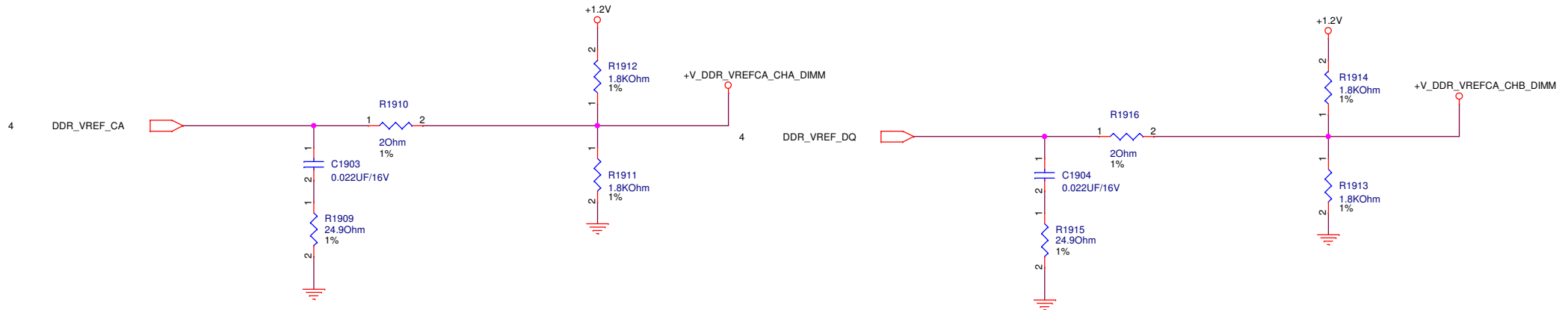




DDR4(3)_CA/DQ Voltage

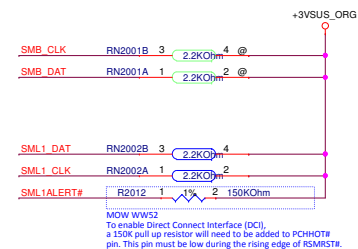
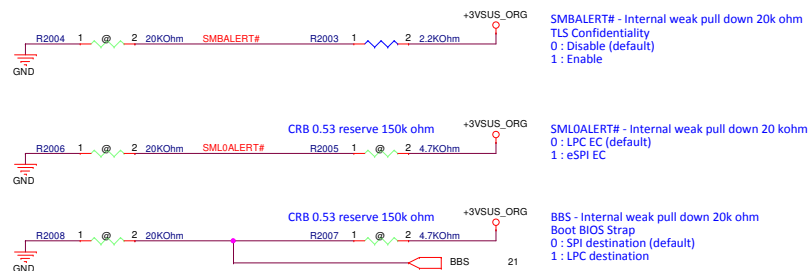
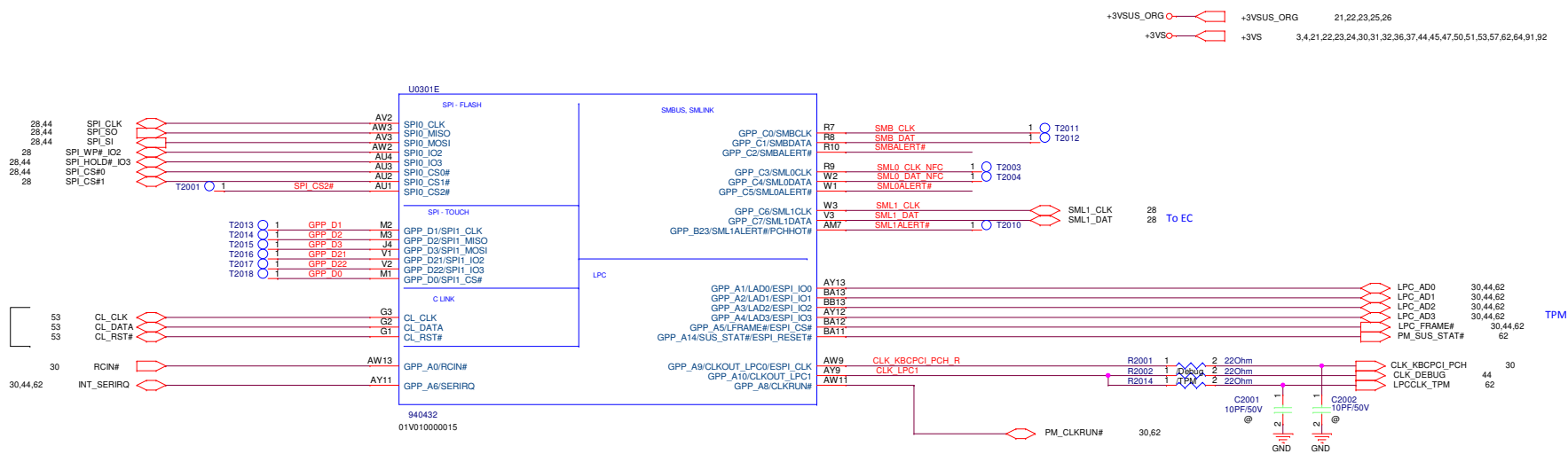
+1.2V 4,7,15,16,17,57,83
+V_DDR_VREFCA_CHB_DIMM
+V_DDR_VREFCA_CHA_DIMM

DDR4 Vref (Intel Schematic Review)



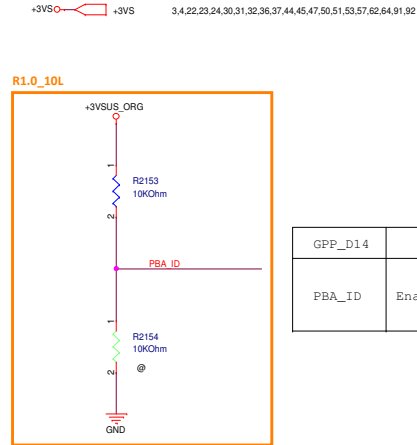
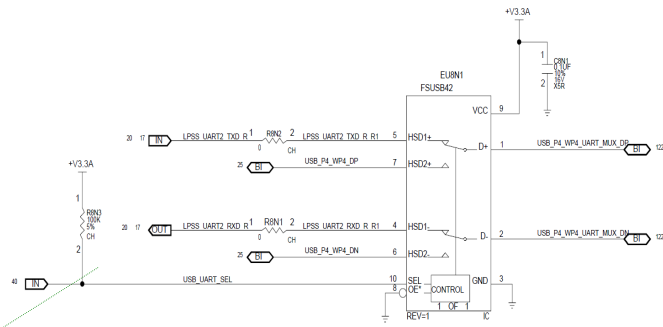
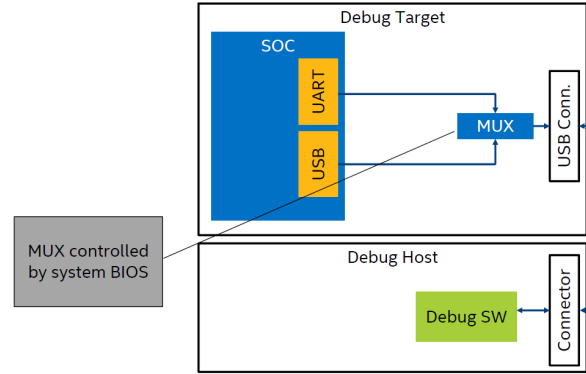
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BG1/HW3			Engineer: Andy Kao		
Size	Project Name				Rev
B	X3				1.0
Date: Wednesday, August 31, 2016			Sheet 19 of 97		

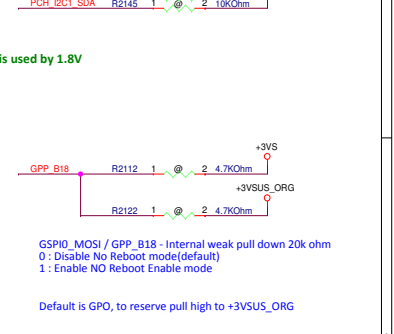
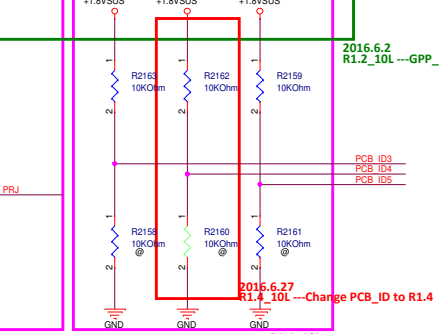
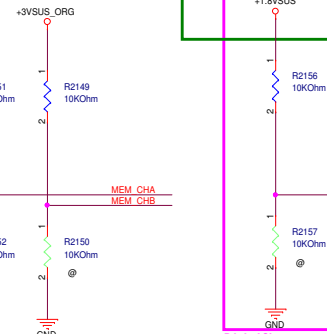
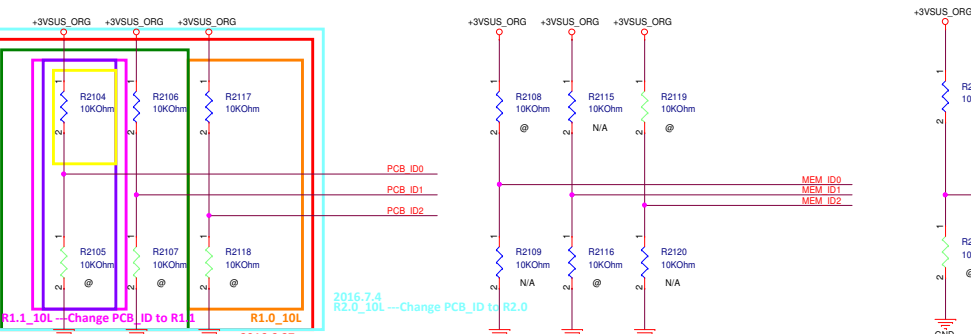
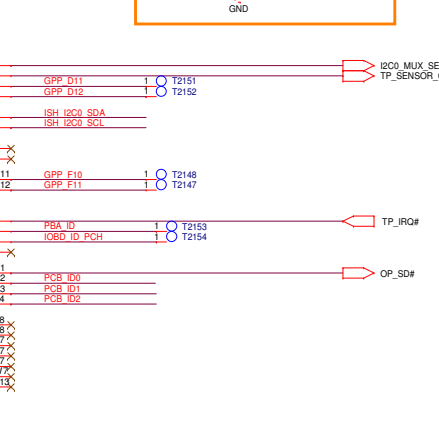
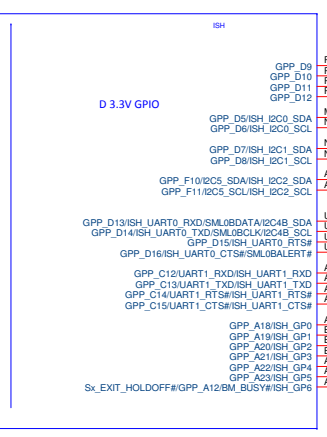
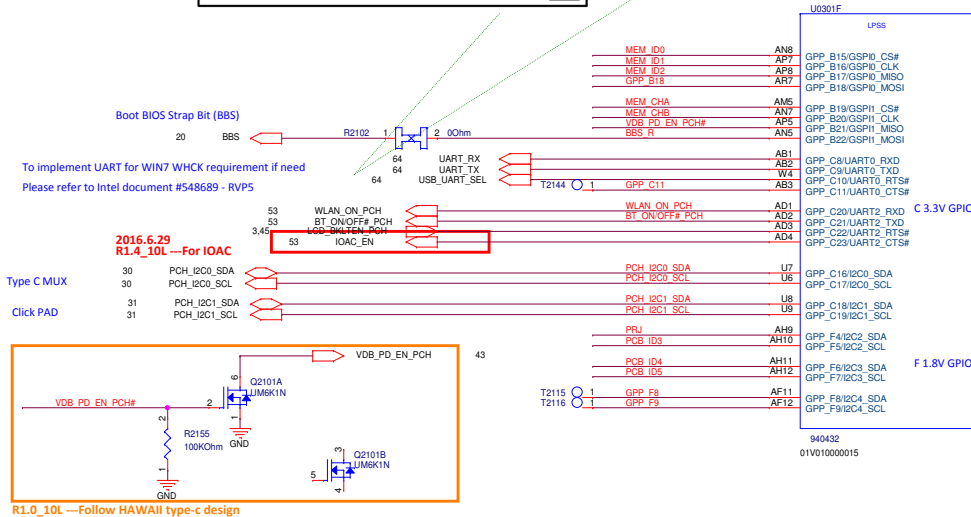


Microsoft* Windows* 7 System WHCK Requirement – OEM platforms are required to include a supported OS debug interface, accessible by an enduser. This allows developers to help in driver debug. The supported Windows 7 debug interfaces are EHCI, 1394 port and COM port.

With skylake EHCI Removal, Potential Gap with Windows* 7 Kernel Debug and OS Installation – Mitigation Required



GPP_D14	1	0
PBA_ID	Enable	Disable



MB Version ID			
PCB_ID4 (GPP_F6)	PCB_ID1 (GPP_C14)	PCB_ID0 (GPP_C13)	
R1.0	0	0	
R1.1	0	1	
R1.2	0	1	
R1.3	0	1	
R1.4	1	0	
R2.0	1	0	
R2.1	1	1	
R2.2	1	1	

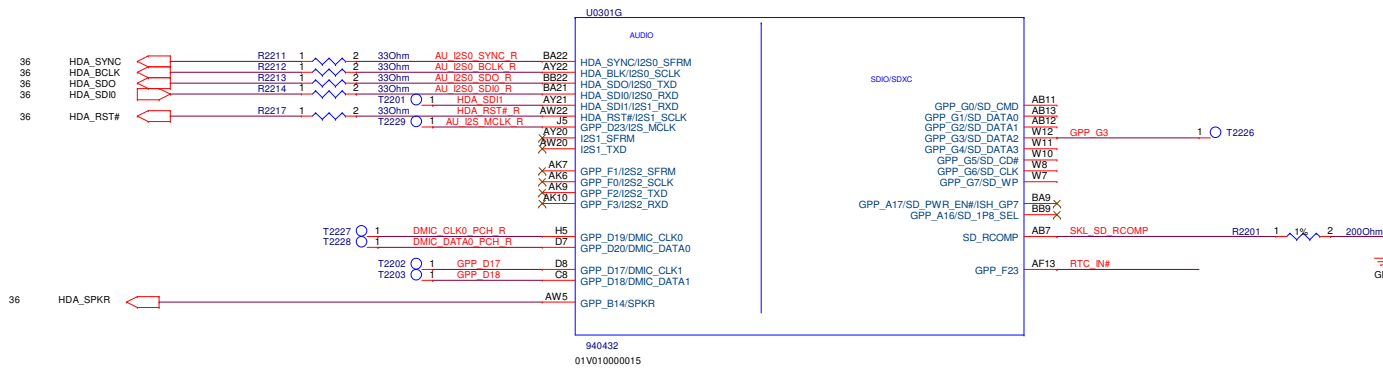
Memory ID			
PCB_ID2 (GPP_C15)	MEM_ID1 (GPP_B16)	MEM_ID0 (GPP_B15)	
8L	0	0	
10L	1	0	
	4Gb	1	
	8Gb	0	
	SAMSUNG	1	
	HYNIX	0	
	MICRON	1	
	RSV	1	

CHA		CHB	
GPP_B19 (0)	Disable		
GPP_B19 (1)	Enable		
GPP_B20 (0)		Disable	
GPP_B20 (1)		Enable	

PRJ	
GPP_F4 (0)	M3
GPP_F4 (1)	X3

PCB_ID3	
GPP_F5 (0)	SKL
GPP_F5 (1)	KBL

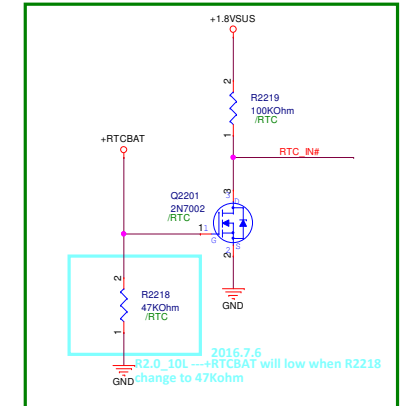
PCB_ID5	
GPP_F7 (0)	2133
GPP_F7 (1)	2400



+VCCPAZIO 26
+3VS 3,4,21,23,24,30,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92
+3VSUS_ORG 20,21,23,25,26

SPKR - Internal weak pull down
0 : Disable TOP Swap mode (default)
1 : Enable Top Swap Enable
Default is GPO, to reserve pull high to +3VSUS_ORG

AU_I2S0_SDO_R - Internal weak pull down
FLASH DESCRIPTOR SECURITY OVERRIDE
0 : Enable security measure defined in the Flash Descriptor
1 : Disable Flash Descriptor Security



2016.5.11
R1.2_10L ---RTC detect circuit

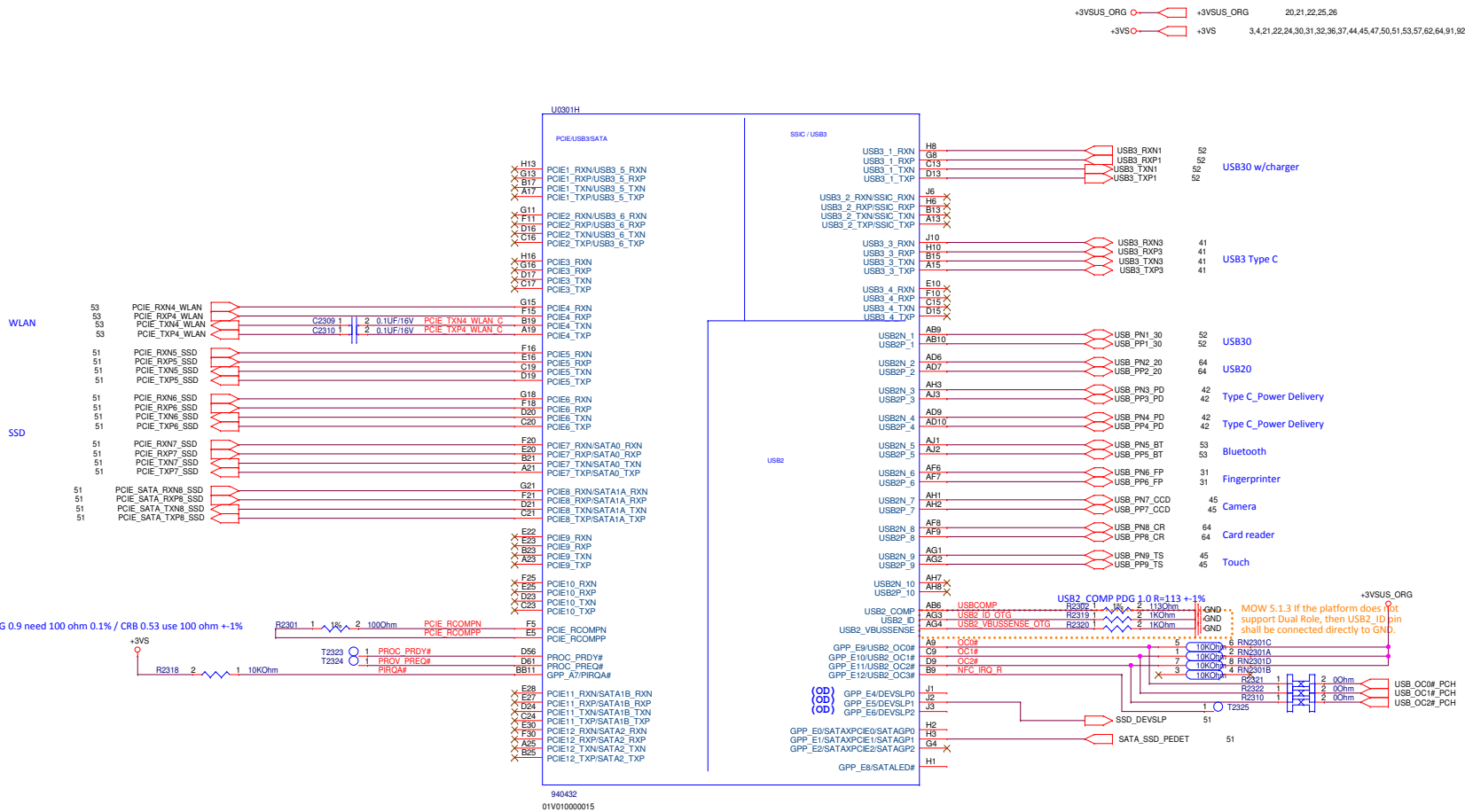


Table 1-2. PCH-LP SKUs (Sheet 2 of 2)

Features	Base-U	Premium-U	Premium-Y
Total Internal RST capable PCIe and SATA Express* Storage Devices	0	2	2
Notes: 1. USB 2.0 port numbers: 1-8 2. USB 2.0 port numbers: 1-10 3. USB 2.0 port numbers: 1-6 4. SATA Express Capable Ports (x2)			

Table 1-3. PCH-LP HSI0 Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0 OTG	USB 3.0 SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	SATA	PCIe	PCIe	PCIe	N/A	N/A
Premium-U	USB 3.0 OTG	USB 3.0 SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe
Premium-Y	USB 3.0 OTG	USB 3.0 SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	N/A	N/A

Capture from 545659_545659_SKL_PCH_LP_EDS_Rev1.0_pub
Please refer the latest Doc.

3.4.1 SKL PCH U Flexible I/O

Figure 3-1. HSI0 Muxing on SKL PCH U

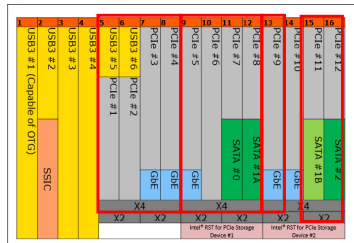
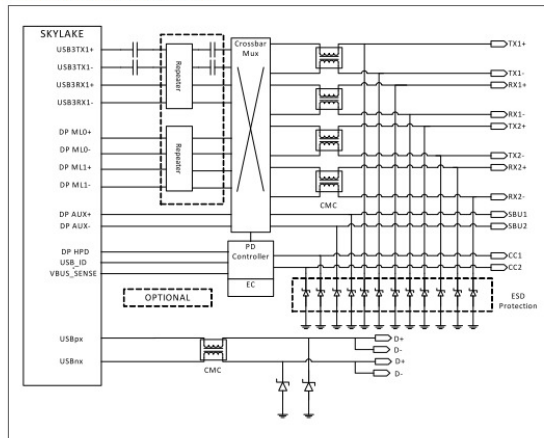
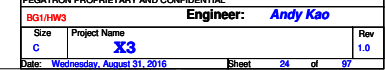


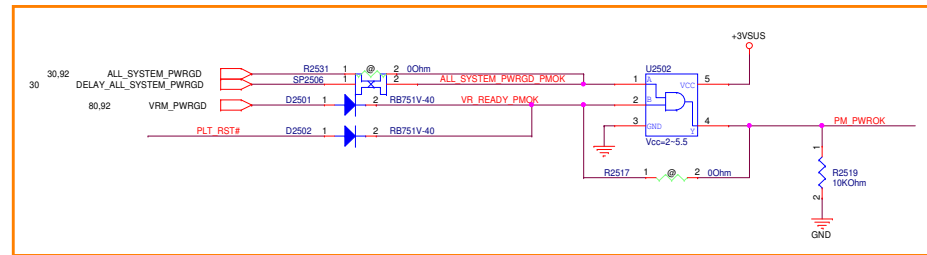
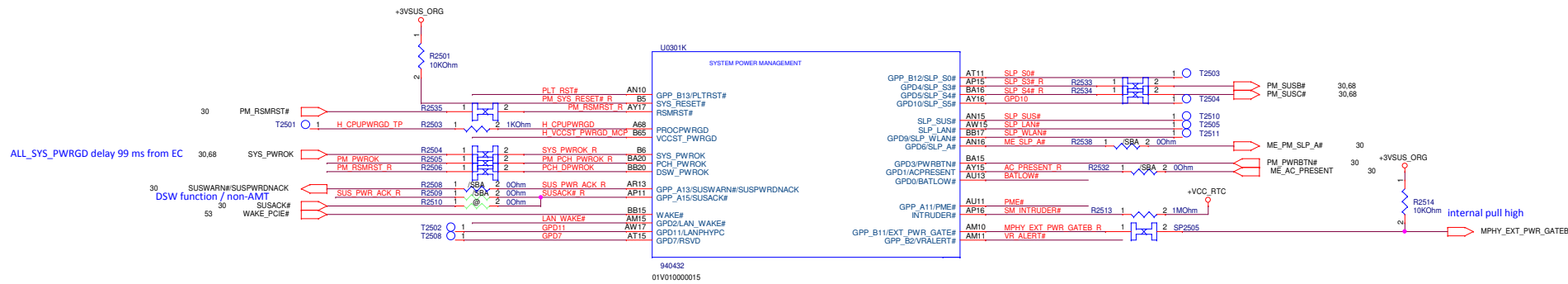
Figure 16-18.USB 3.0 Dual Role and DP x 2



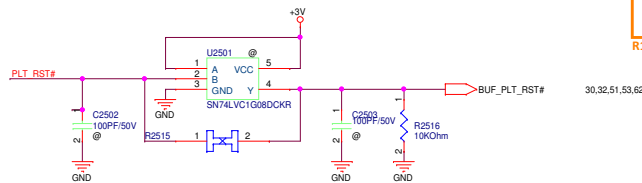
Note: The figure above is a high level example implementation block; actual implementation on schematic may vary.



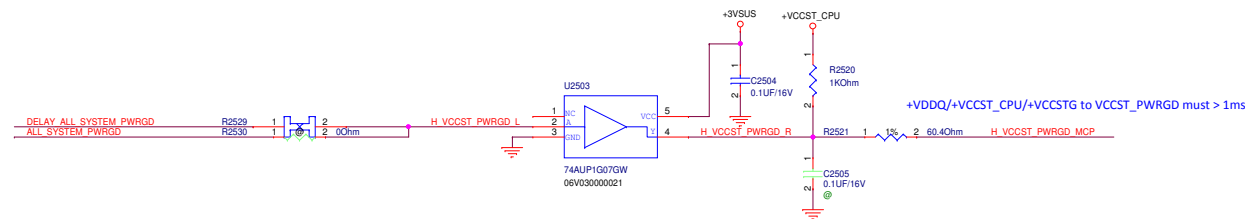
+3VSUS_ORG		+3VSUS_ORG	20,21,22,23,26
+VCC_RTC		+VCC_RTC	24,26,36,60
+VCCDSW		+VCCDSW	26,30
+VCCST_CPU		+VCCST_CPU	3,5,7,9,32
+3V		+3V	31,57,82,91
+3VSUS		+3VSUS	4,24,26,28,30,31,41,42,51,53,62,64,68,81,92

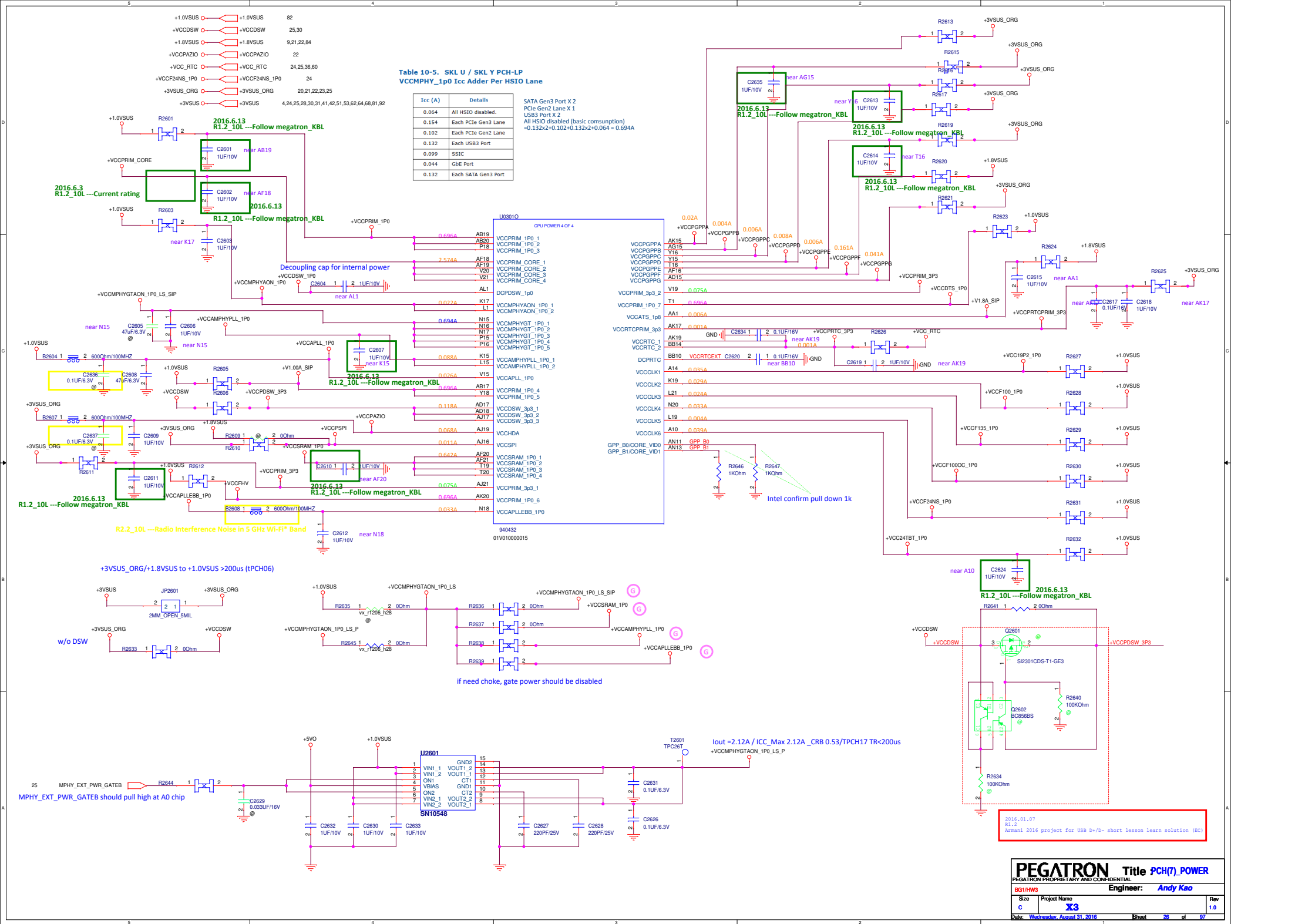


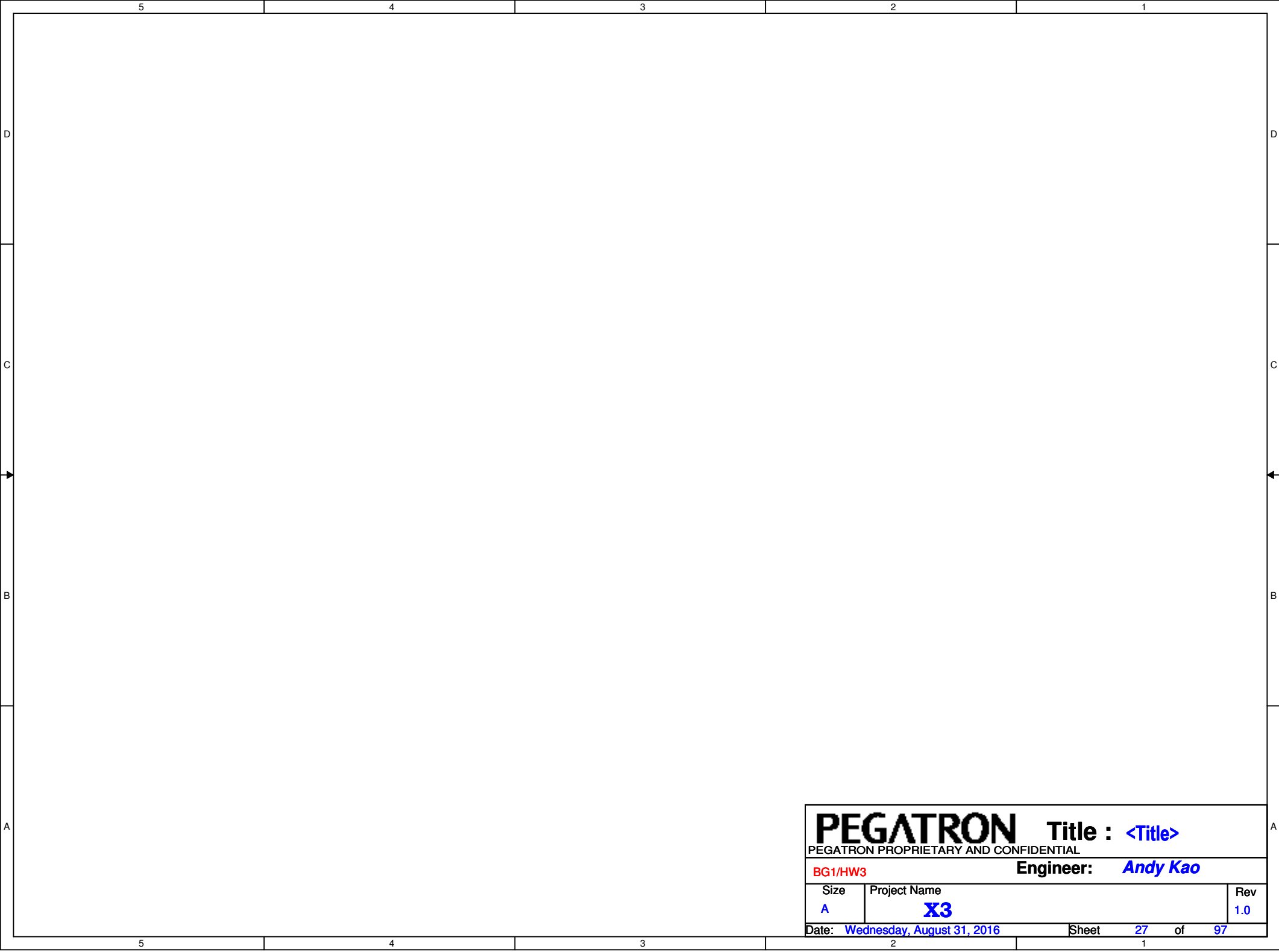
R1.0_10L ---Shutdown possible solution



EC delay ALL_SYSTEM_PWRGD 2ms

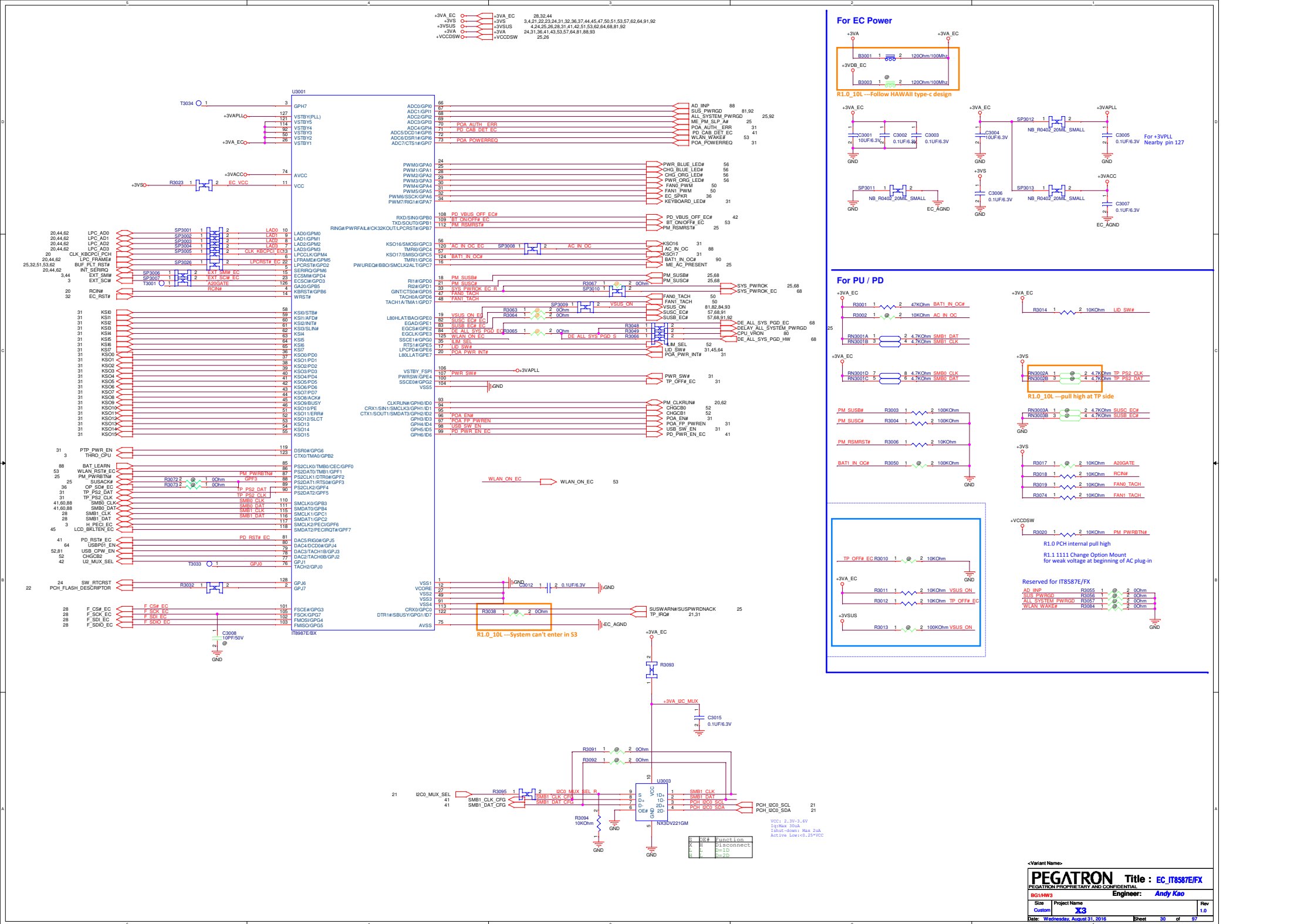


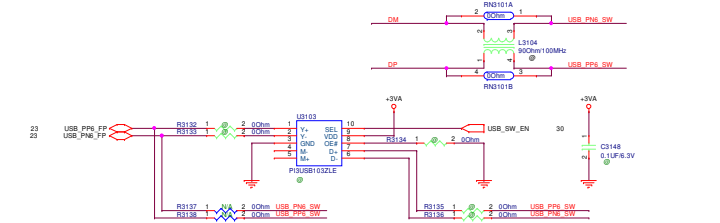
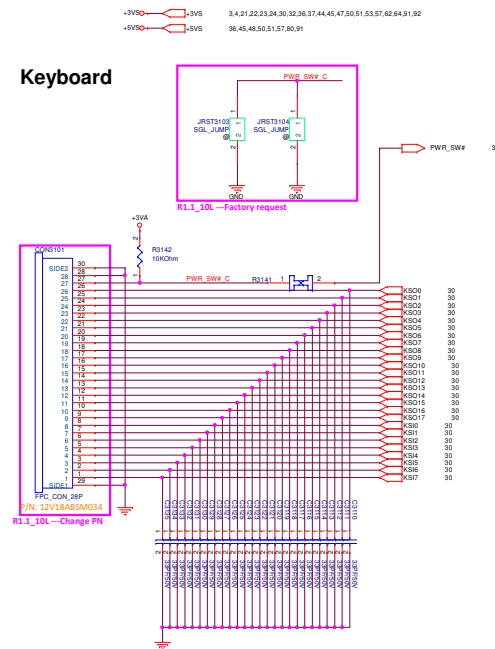




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BG1/HW3		Engineer: <i>Andy Kao</i>
Size <i>A</i>	Project Name X3	Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>27</i> of <i>97</i>

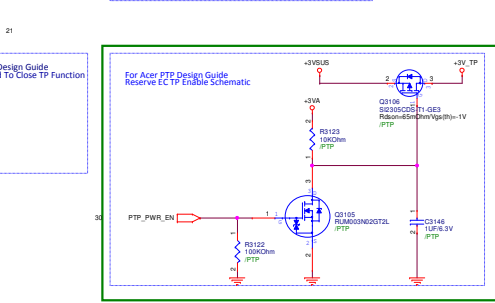
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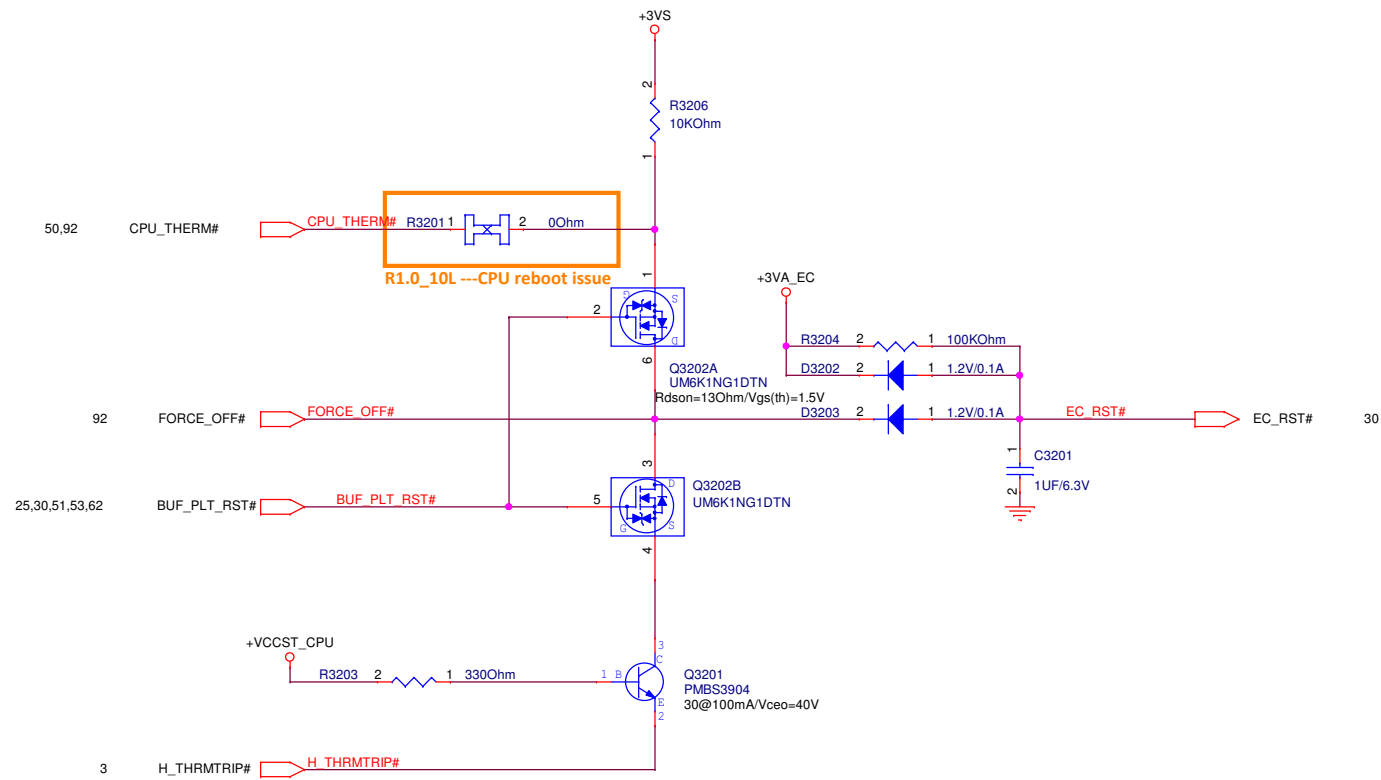


[illegible][illegible]

2016.6.3
R1.2_10L ---Win7 TP issue

The diagram shows a circuit connection between a +3V pin and a -3V TP pin. The connection is made through two resistors, RS11182 and RS11172, each with a value of 1000m. The resistors are connected in series. The diagram is enclosed in a green box, and a blue dashed box labeled "Touch Pad Wake Up S3" is connected to the bottom of the resistors.





PEGATRON		Title : <i>RST_Reset Circuit</i>
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BG1/HW3		Engineer: <i>Andy Kao</i>
Size B	Project Name X3	Rev 1.0
Date: Wednesday, August 31, 2016		Sheet 32 of 97

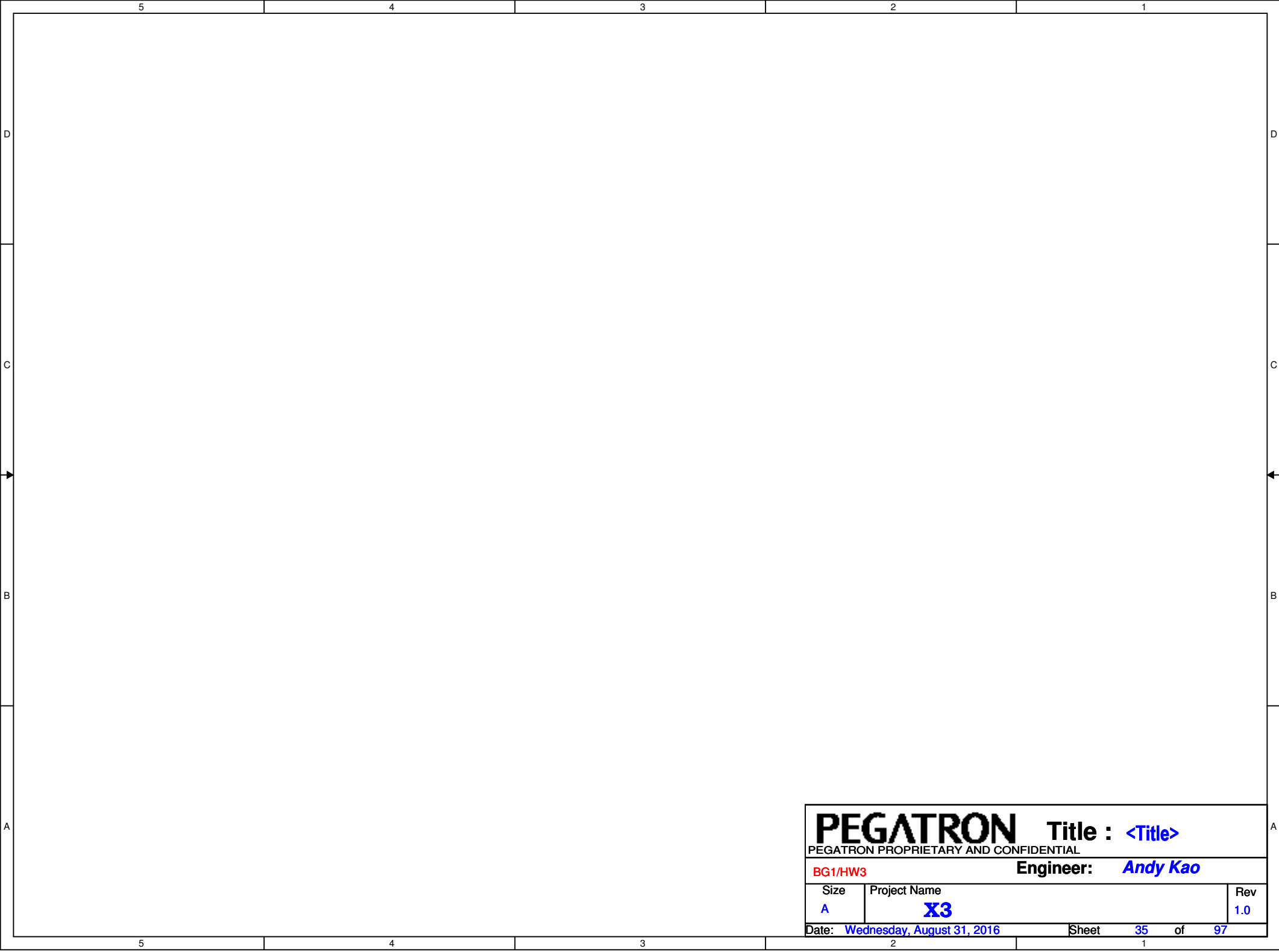
PEGATRON Title : [<Title>](#)

BG1/HW3 **Engineer:** *Andy Kao*

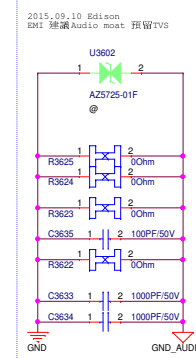
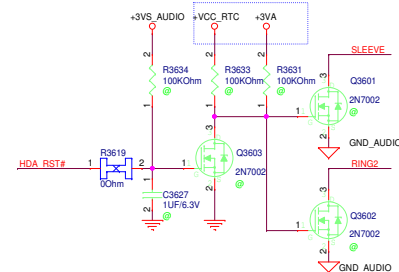
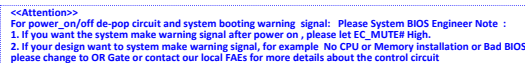
Size A	Project Name X3	Rev 1.0
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Date: Wednesday, August 31, 2016	Sheet 33 of 97
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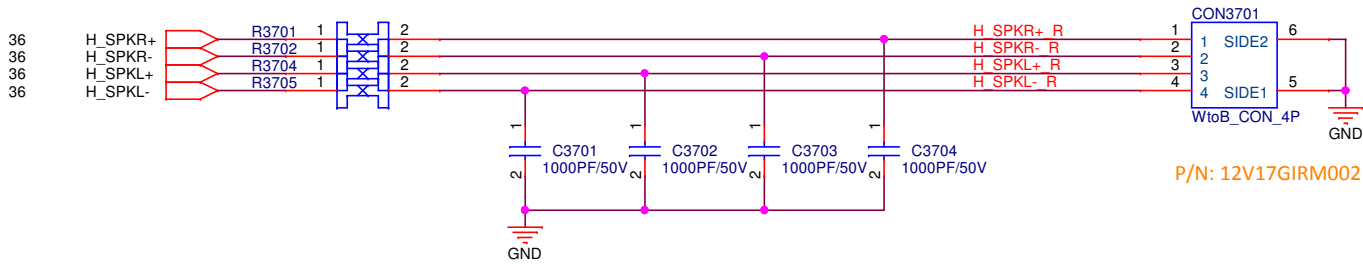
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PEGATRON										Title : <Title>																																																																																																								
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Date: Wednesday, August 31, 2016										Sheet 34 of 97																																																																																																								
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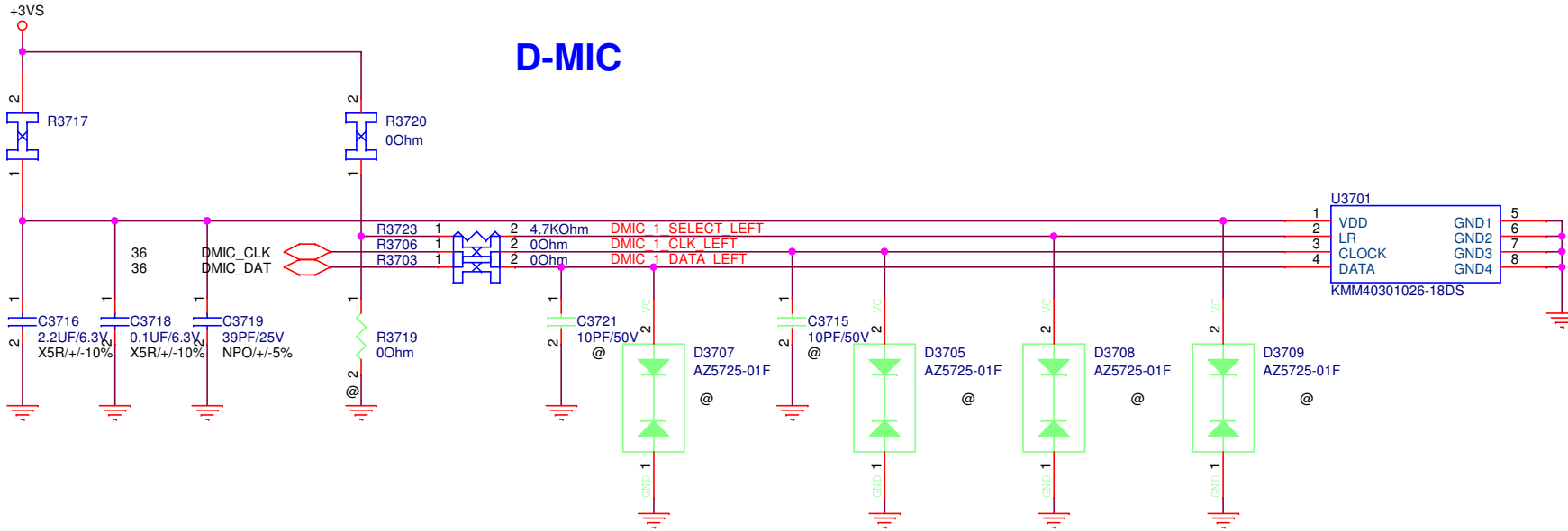
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size A	Project Name X3		Rev 1.0
Date: Wednesday, August 31, 2016		Sheet 35 of 97	

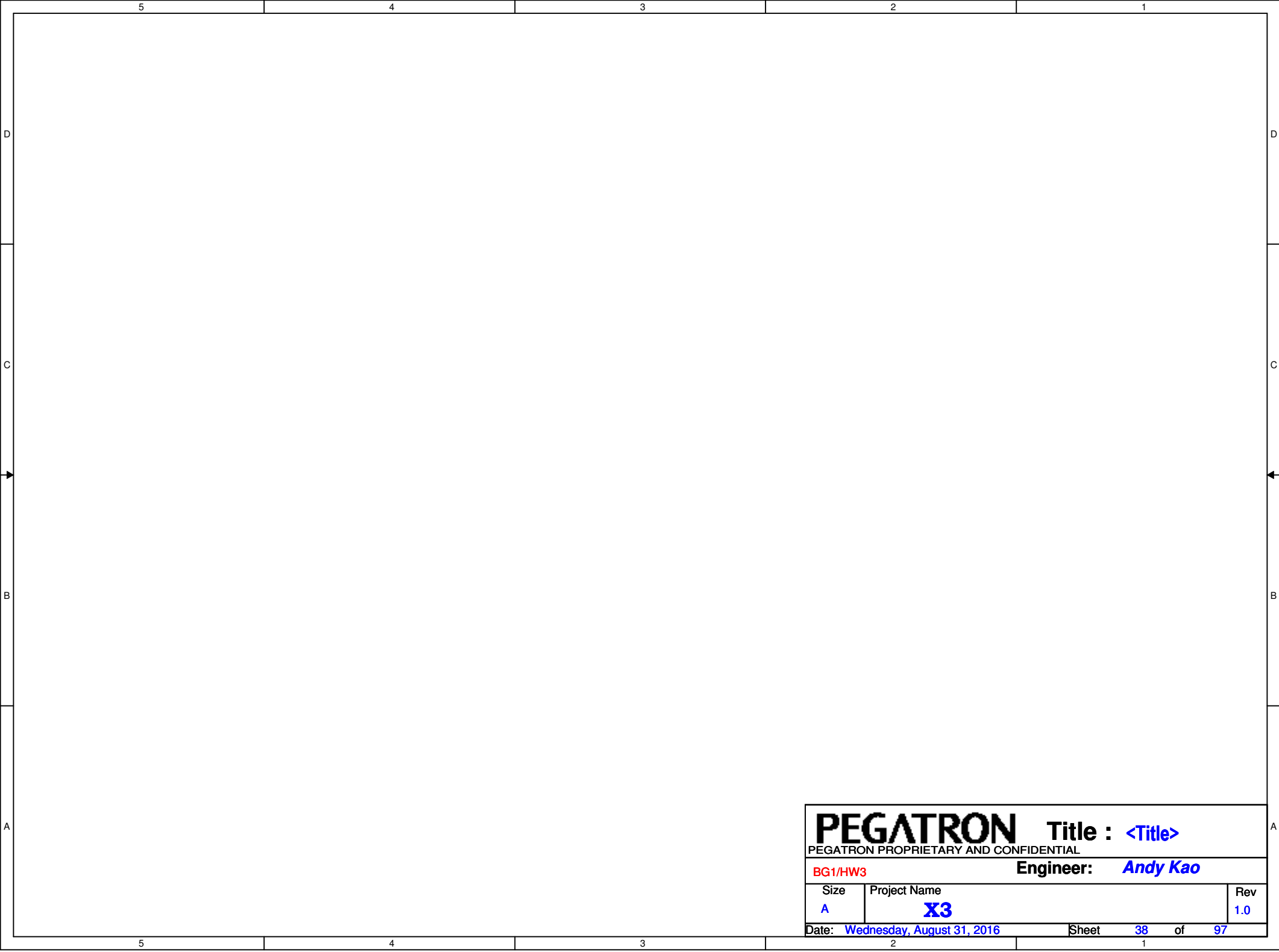


Speaker

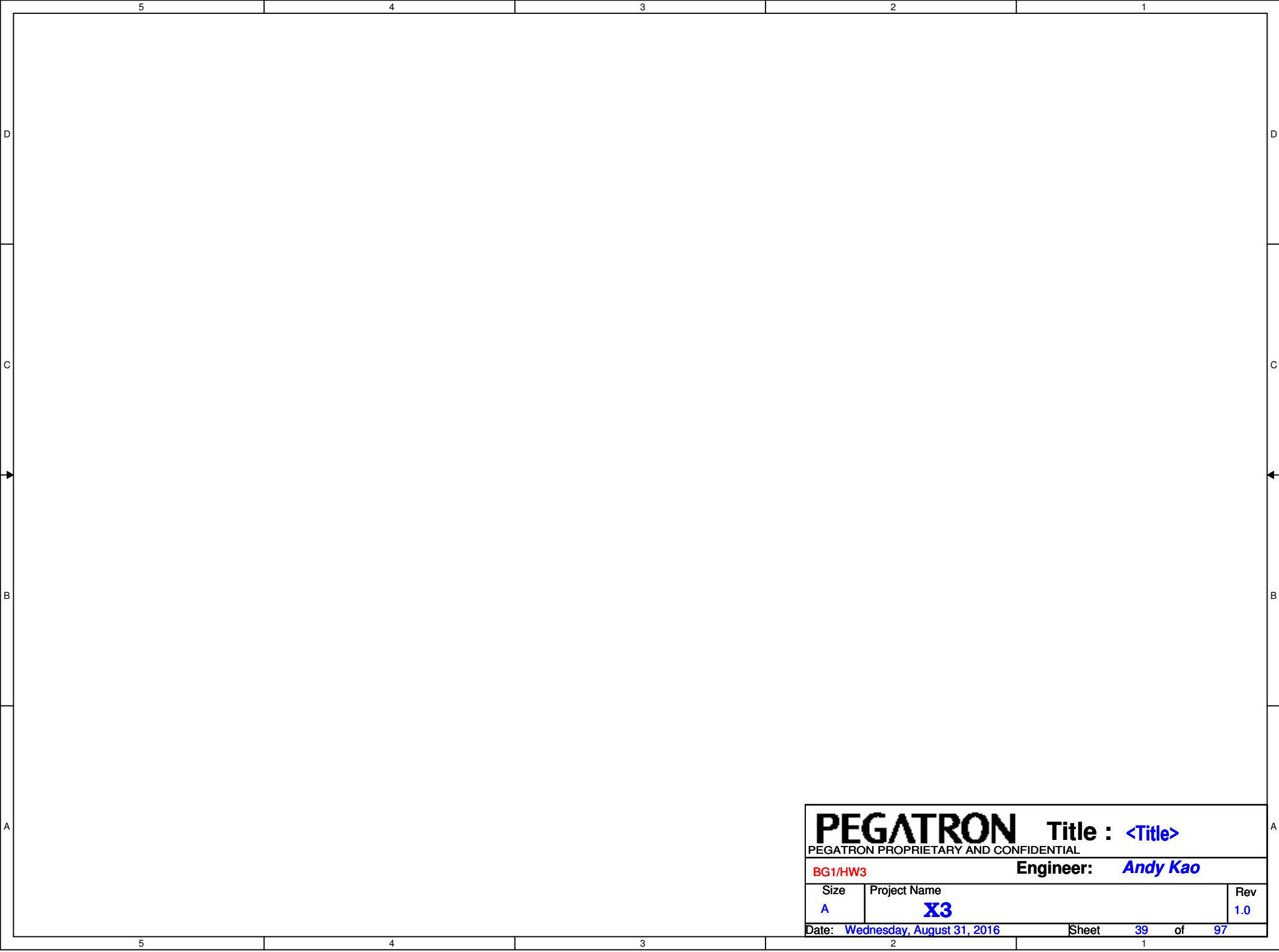


D-MIC



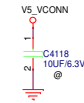
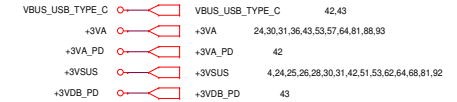
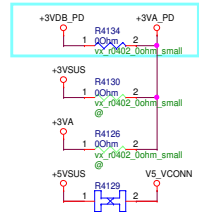


PEGATRON		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size <i>A</i>	Project Name X3		Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>38</i> of <i>97</i>	



PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size <i>A</i>	Project Name X3	Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>39</i> of <i>97</i>

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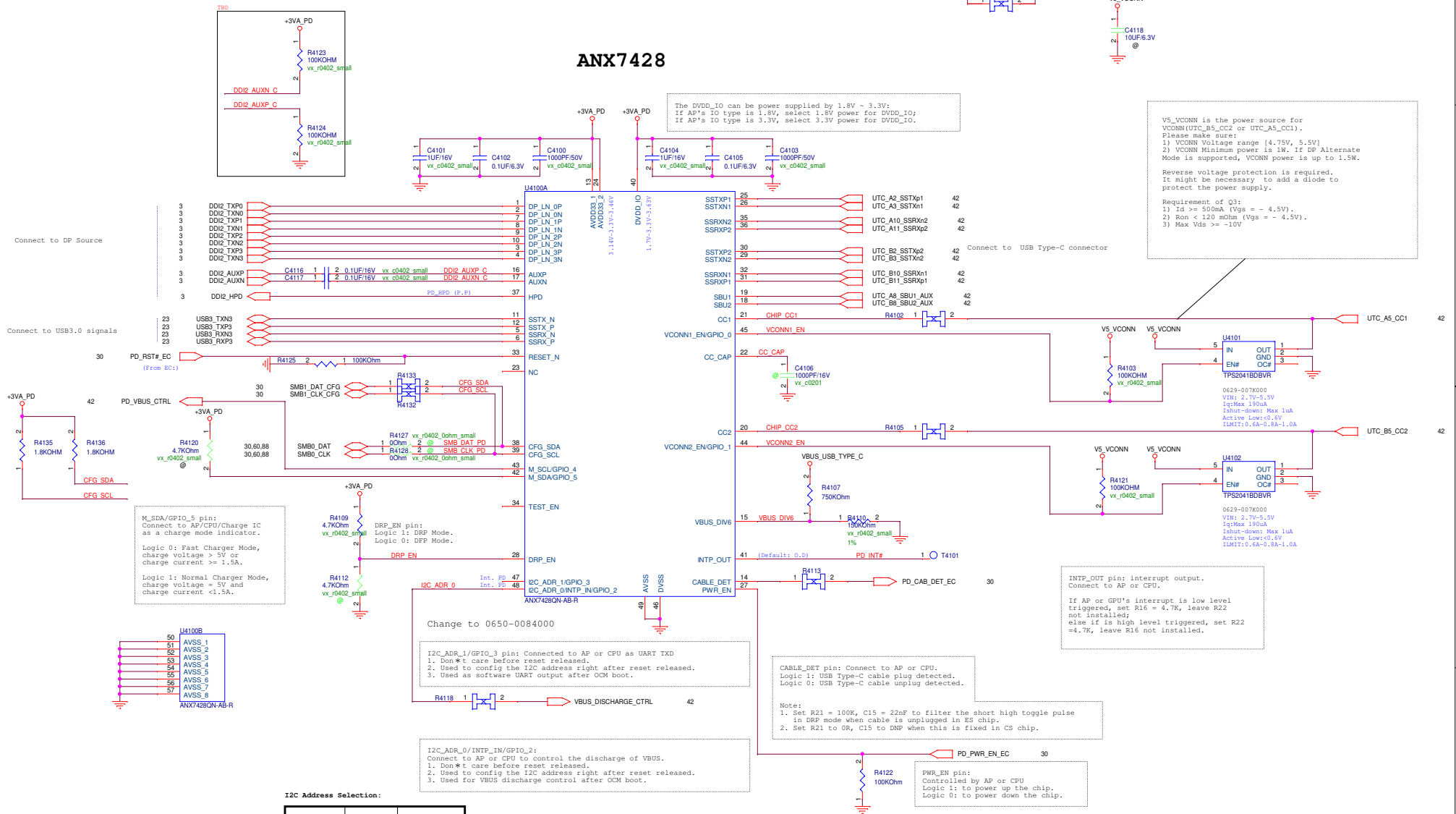
V5_VCONN is the power source for VCONN(UTC_B5_CC2 or UTC_A5_CC1). Please make sure:

- 1) VCONN Voltage range [4.75V, 5.5V]
- 2) VCONN Minimum power is 1W. If DP Alternate Mode is supported, VCONN power is up to 1.5W.

Reverse voltage protection is required. It might be necessary to add a diode to protect the power supply.

Requirement of Q3:

- 1) $I_d \geq 500\text{mA}$ ($V_{gs} = -4.5\text{V}$).
- 2) $R_{on} < 120\text{ m}\Omega$ ($V_{gs} = -4.5\text{V}$).
- 3) $\text{Max } V_{ds} \geq -10\text{V}$



I2C_ADR_1	I2C_ADR_0	I2C Address
Logic 0	Logic 0	0x50
Logic 0	Logic 1	0x72
Logic 1	Logic 0	0x7c
Logic 1	Logic 1	0x80

1. The I2C address is determined approximately 500ns after RESET_N turns from 0 to 1, the I2C pin I2C_ADDR_0 should be kept at a stable value during this period.
2. There are internal pull-down resistors on I2C_ADDR_0 and I2C_ADDR_1 pins.
3. If external pull-up resistor is not populated, the I2C_ADDR_0 or I2C_ADDR_1 is logic 0.
4. If external pull-up is populated, the I2C_ADDR_0 or I2C_ADDR_1 is logic 1.

<Variant Name>

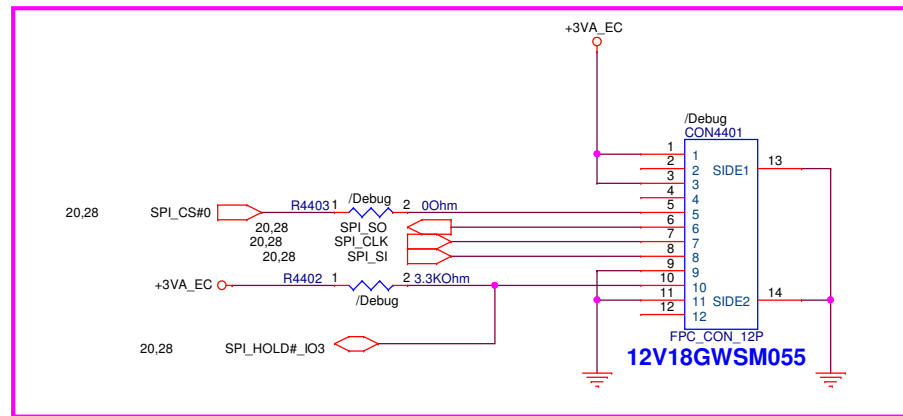
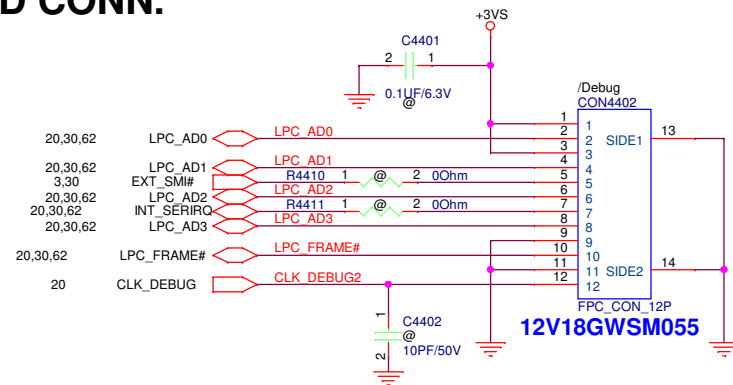
PEGATRON Title : POWER_FLOWCHART
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: **Andy Kao**

Size C	Project Name X3	Rev 1.0
Date: Wednesday, August 31, 2016 Sheet 41 of 97		

<div> <div><Variant Name></div> <div> <div>PEGATRON</div> <div> <div>REGISTRAR/POWERFLOWCHART AND CONFIGURE</div> </div> </div> </div>		<div> <div>Title</div> <div>POWER_FLOWCHART</div> </div>
<div> <div>Engineer:</div> <div>Andy Kao</div> </div>		
<div> <div>Size</div> <div>D</div> </div>	<div> <div>Project Name</div> <div>X3</div> </div>	<div> <div>Rev</div> <div>1.0</div> </div>
<div> <div>Date:</div> <div>Wednesday, August 31, 2016</div> </div>	<div> <div>Sheet</div> <div>42</div> </div>	<div> <div>of</div> <div>97</div> </div>

DEBUG CARD CONN.

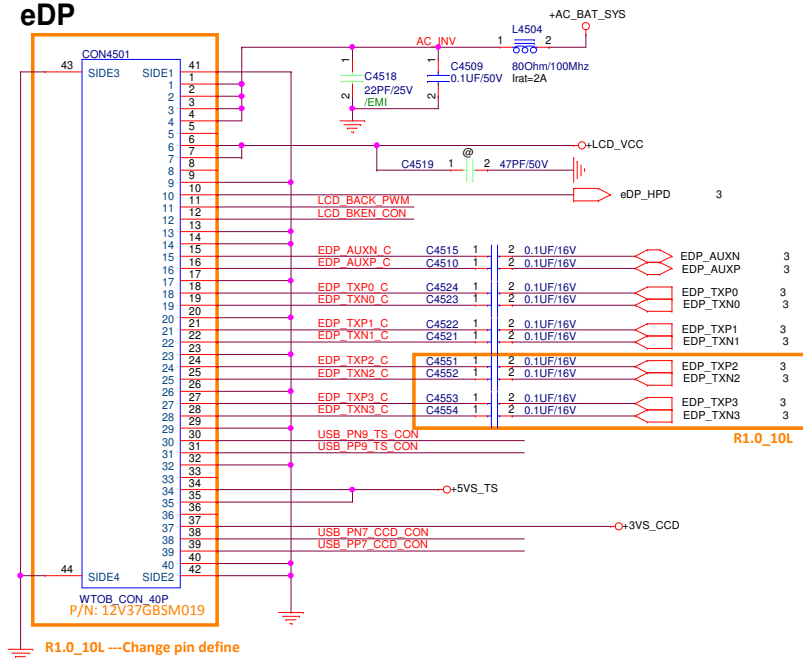


R1.1_10L ---BIOS request

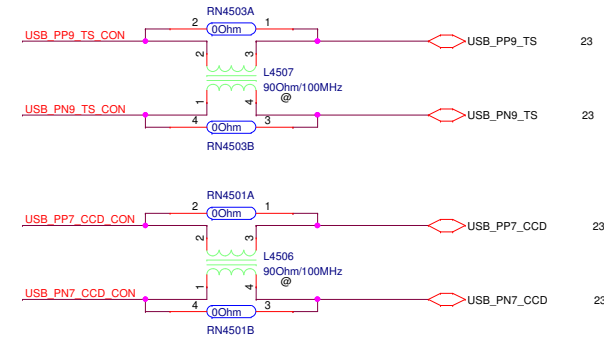
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PEGATRON		Title : DEBUG CONN.	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Andy Kao	
Size B	Project Name X3		Rev 1.0
Date: Wednesday, August 31, 2016		Sheet 44 of 97	

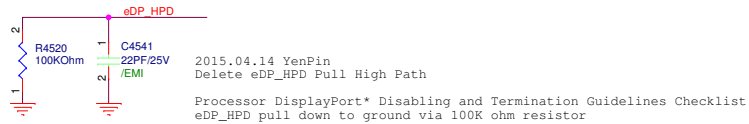
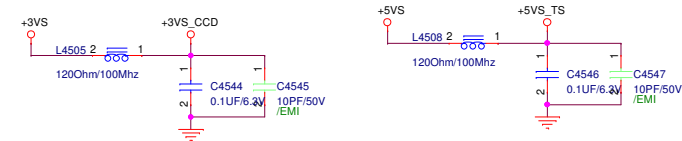
eDP



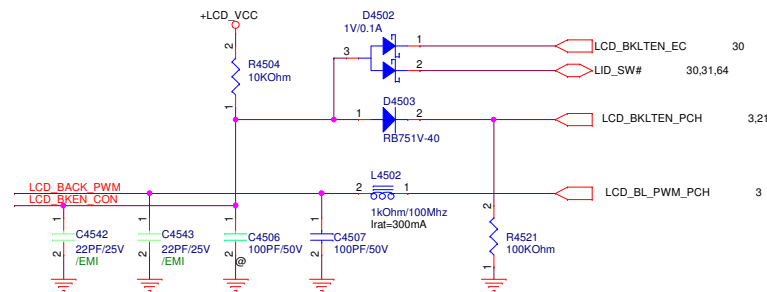
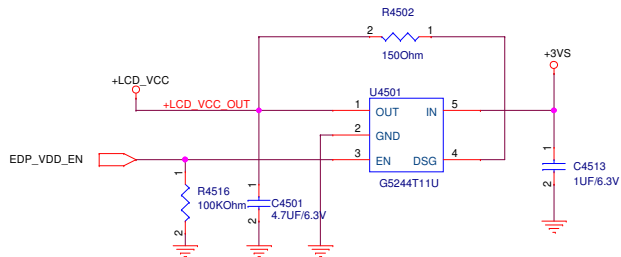
+3VS	+3VS	3,4,21,22,23,24,30,31,32,36,37,44,47,50,51,53,57,62,64,91,92
+5VS	+5VS	31,36,48,50,51,57,80,91
+AC_BAT_SYS	+AC_BAT_SYS	43,80,81,82,83,88



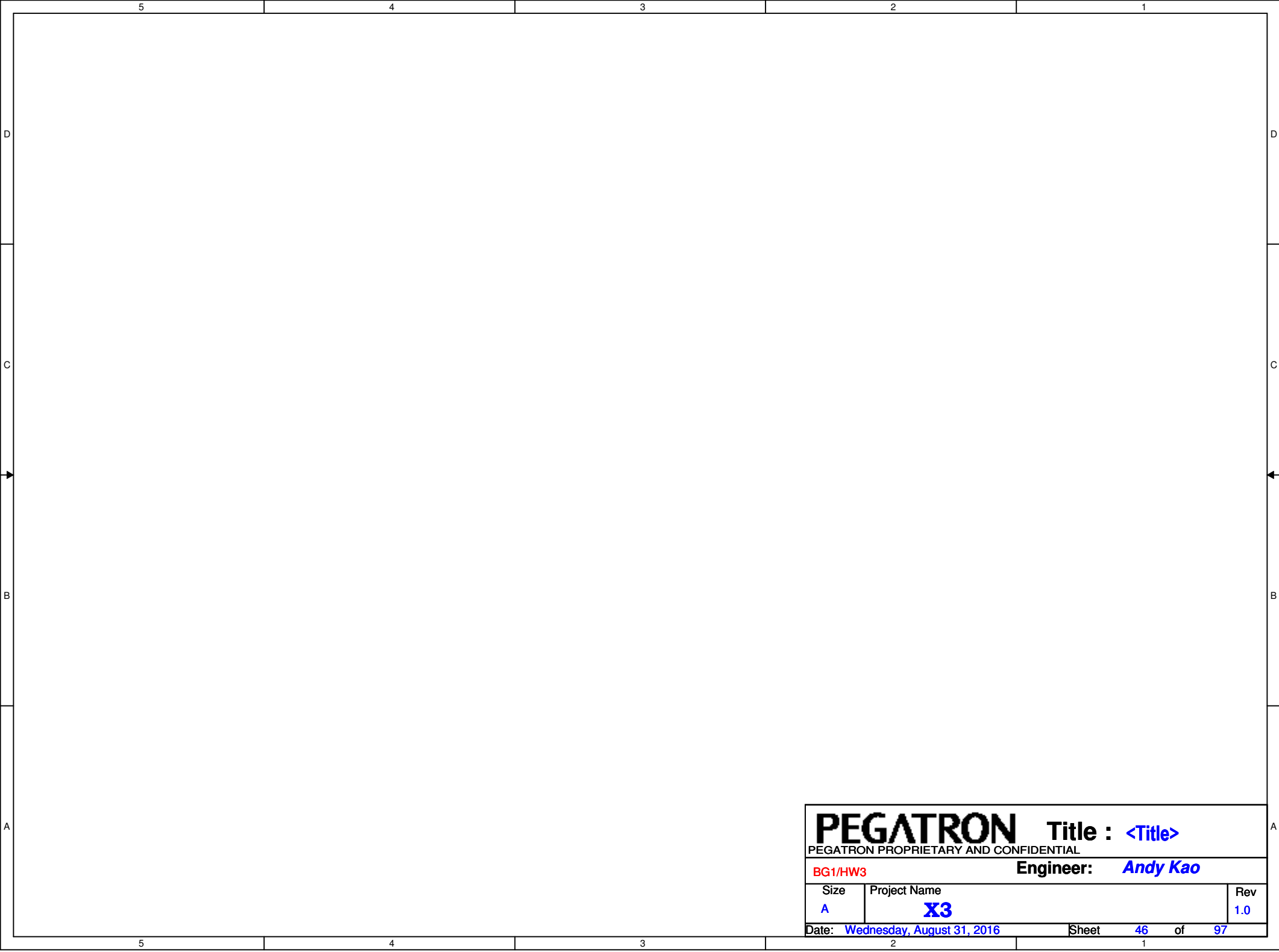
Camera



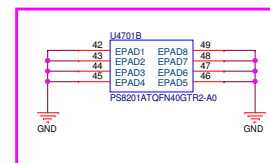
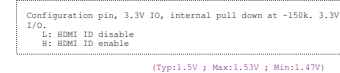
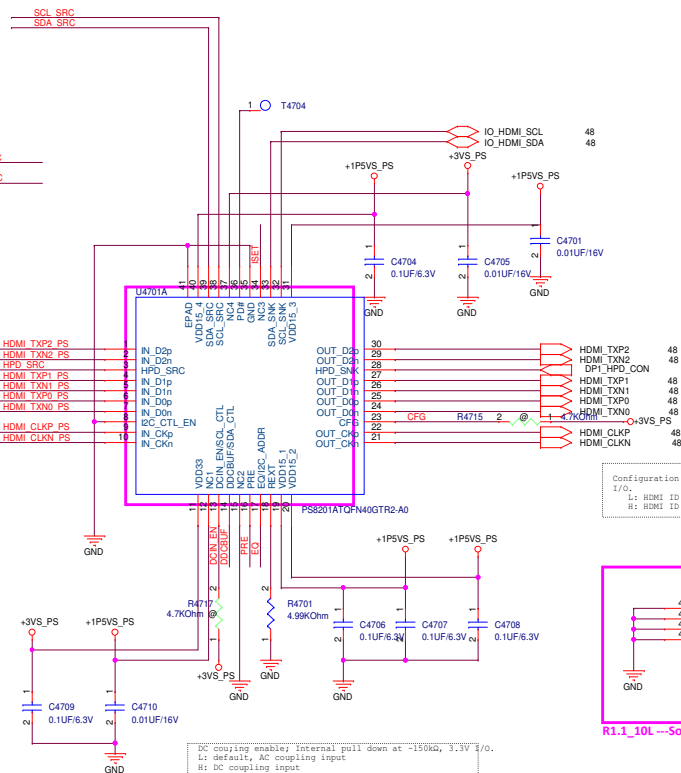
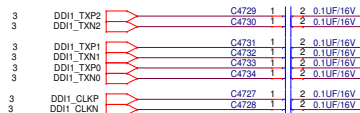
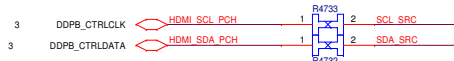
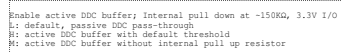
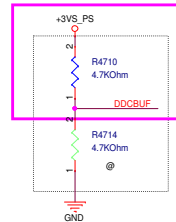
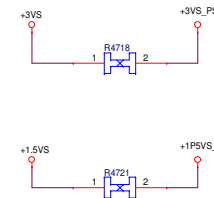
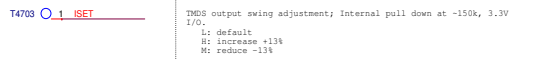
LCD VDDEN / +LED_VCC



<Variant Name>		Title : eDP CONN	
Size	Project Name	Engineer: Andy Kao	Rev
Custom	X3		1.0
Date: Wednesday, August 31, 2016	Sheet 45 of 97		



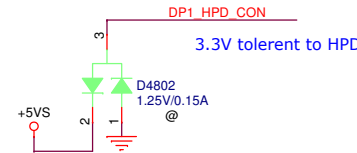
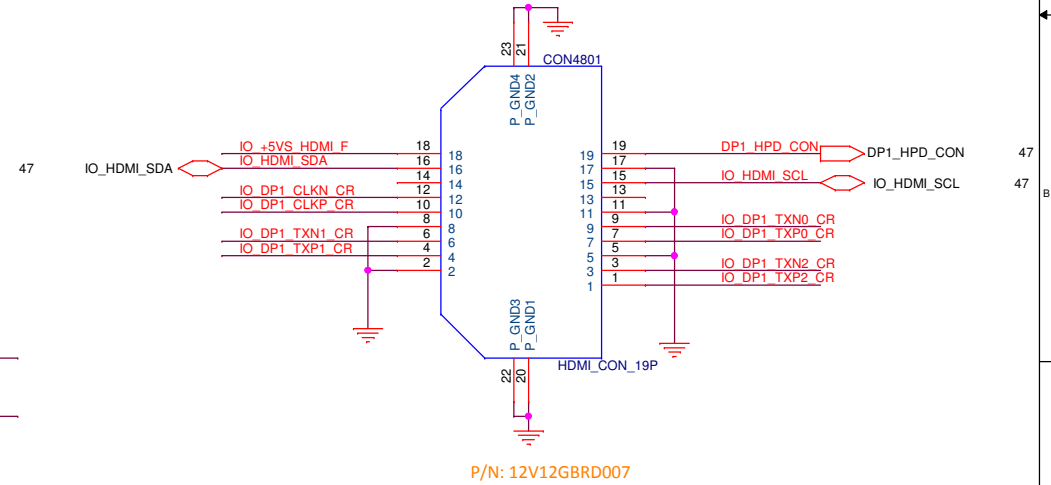
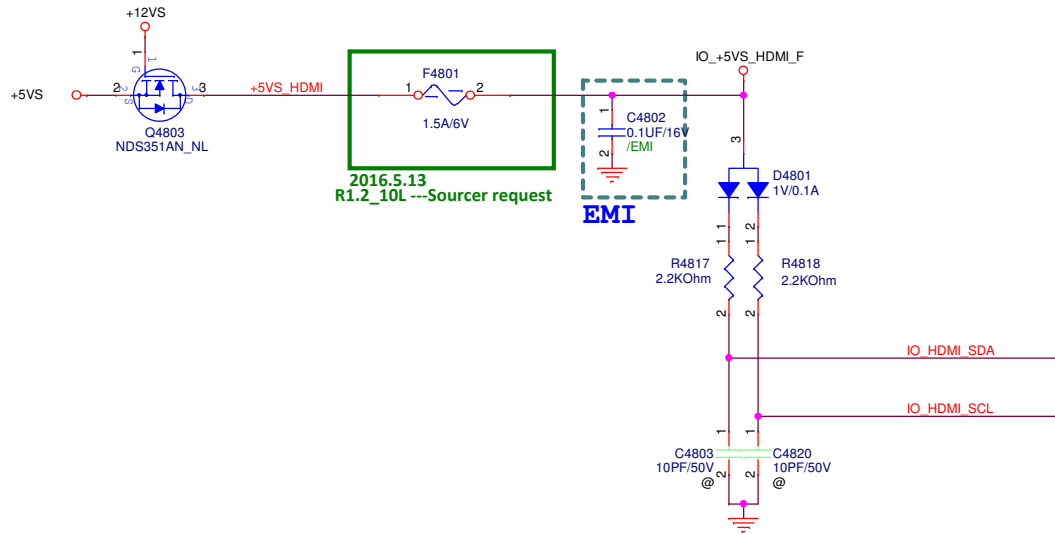
PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size A	Project Name X3	Rev 1.0
Date: Wednesday, August 31, 2016		Sheet 46 of 97



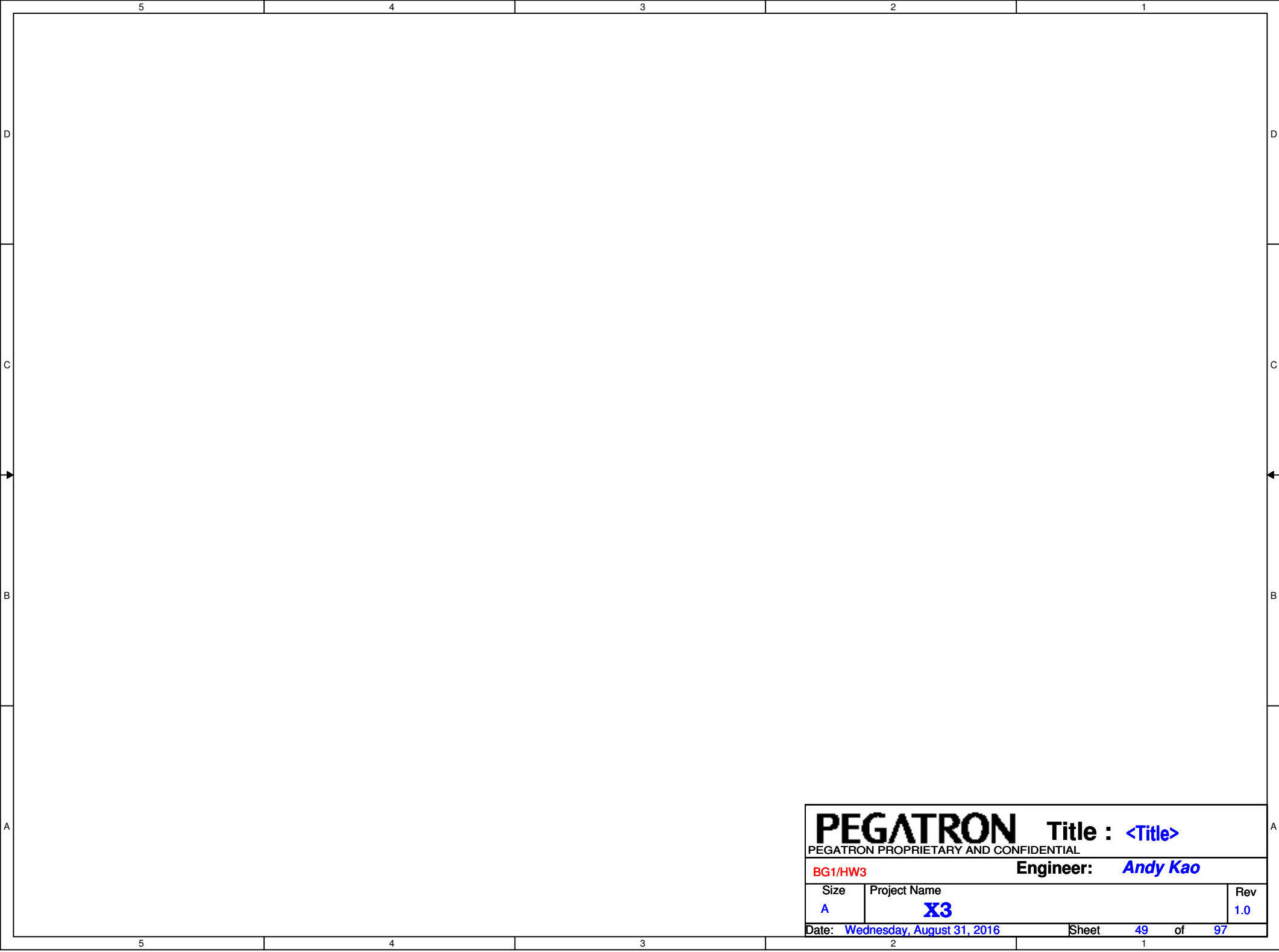
R1.1 10L ---Sourcer request

HDMI

+3VS	+3VS	3,4,21,22,23,24,30,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92
+5VS	+5VS	31,36,45,50,51,57,80,91
+12VS	+12VS	31,57,91



PEGATRON		Title : HDMI-4K2K	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Andy Kao	
Size B	Project Name X3		Rev 1.0
Date: Wednesday, August 31, 2016		Sheet 48	of 97

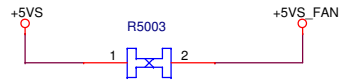
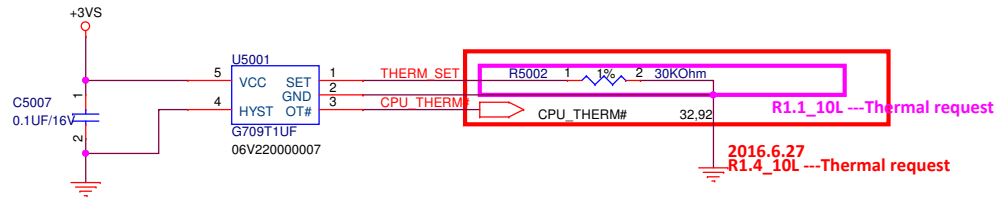


PEGATRON		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size <i>A</i>	Project Name X3		Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>49</i> of <i>97</i>	

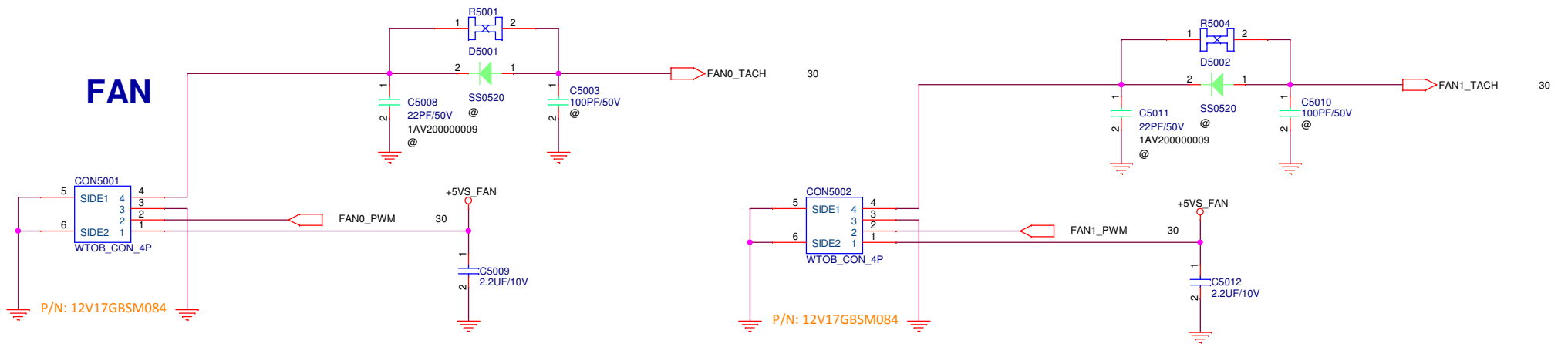
Thermal Sensor

```
temp setting : 80 degree
```

$$R_{SET}(k\Omega) = 0.0012T^2 - 0.9308T + 96.147$$



FAN



<Variant Name>

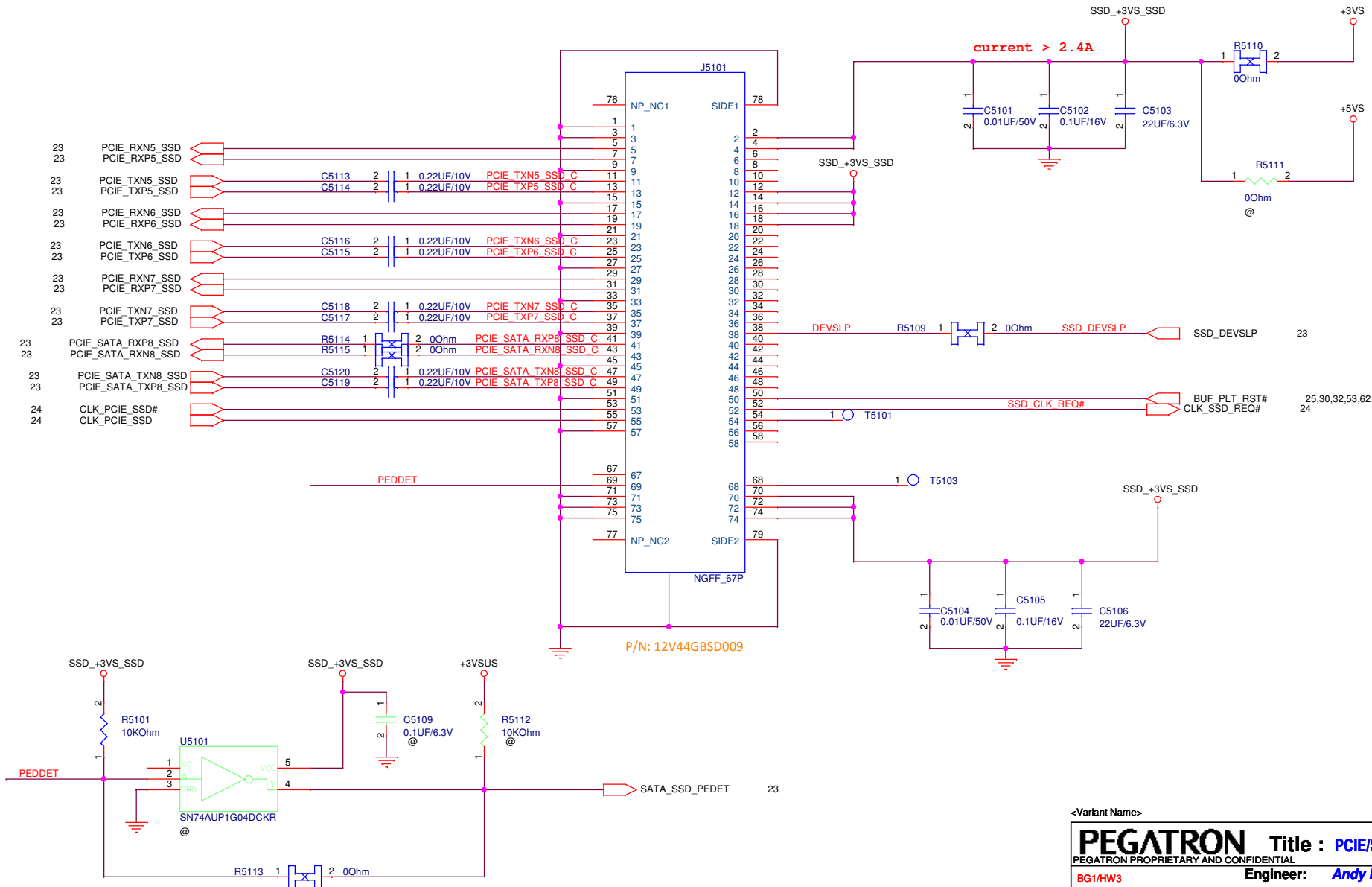
PEGATRON Title : Thermal/Fan

BG1/HW3 Engineer: *Andy Kao*

Size	Project Name	Rev
B	X3	1.0

Date: **Wednesday, August 31, 2016** Sheet **50** of **97**

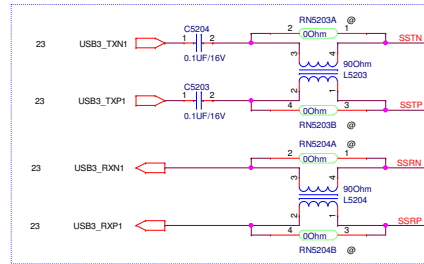
SSD(SATA/PCIE x4) NGFF socket (M-key)



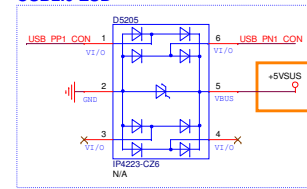
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PEGATRON Title : PCIE/SATA SSD		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: Andy Kao
Size	Project Name	Rev
Custom	X3	1.0
Date: Wednesday, August 31, 2016	Sheet 51 of 97	

USB 3.0

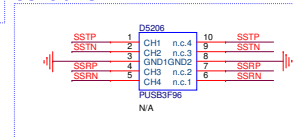
USB3.0 Choke



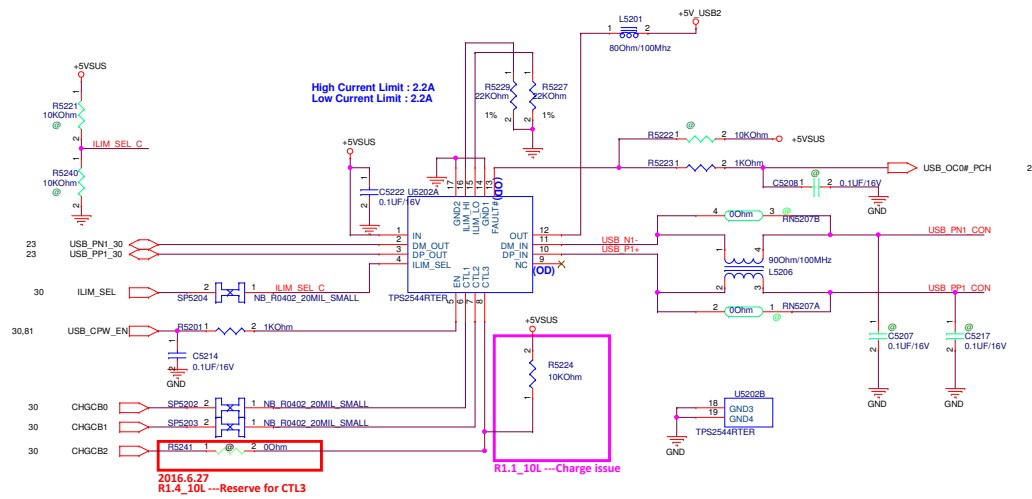
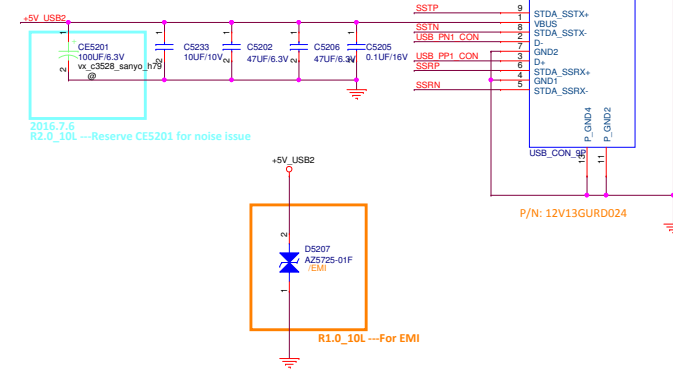
USB2.0 ESD



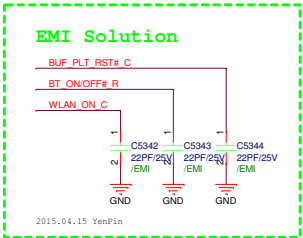
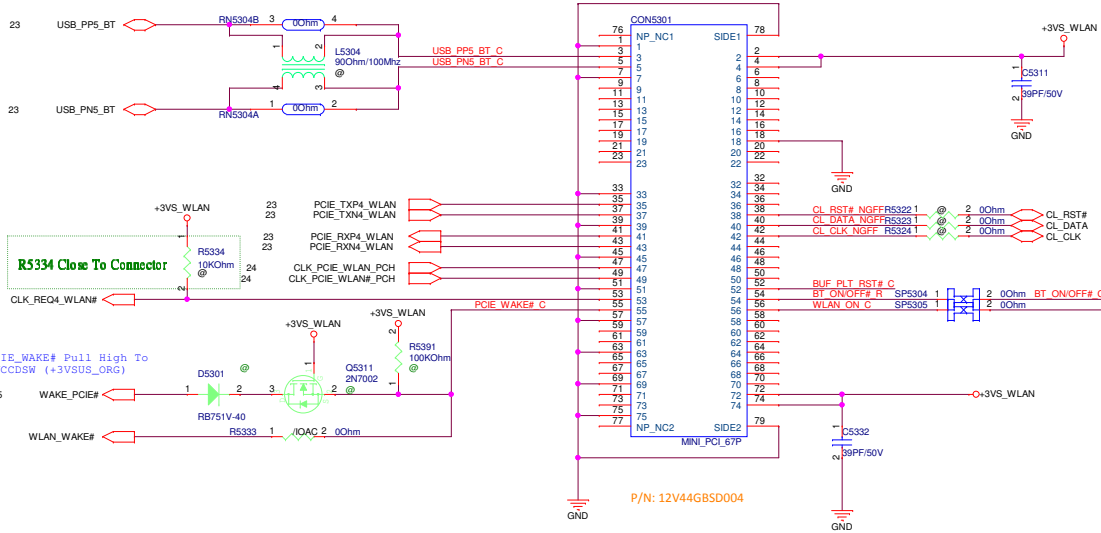
USB3.0 ESD



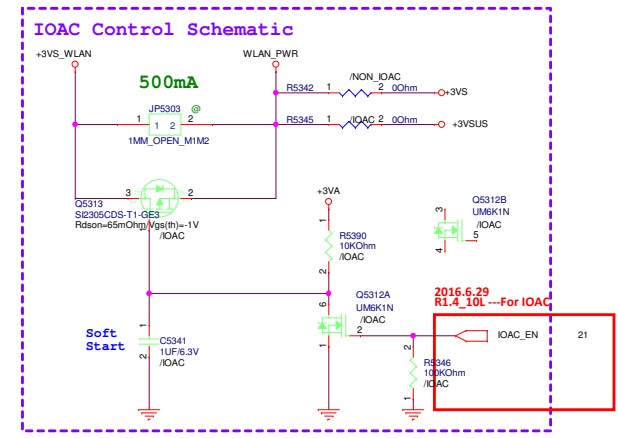
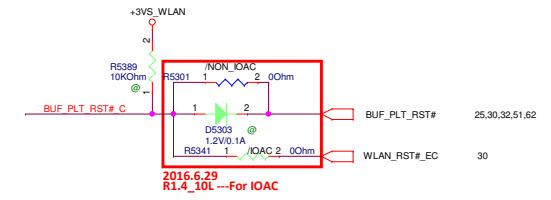
USB 3.0 - Type A



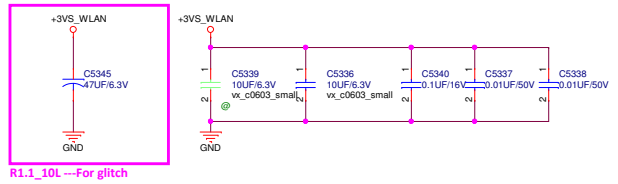
WLAN/BT with NGFF socket E



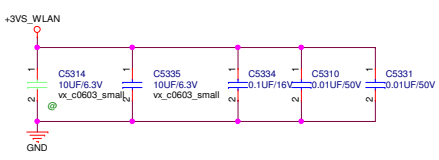
+3VS 3.4,21,22,23,24,30,31,32,36,37,44,45,47,50,51,57,62,64,91,92



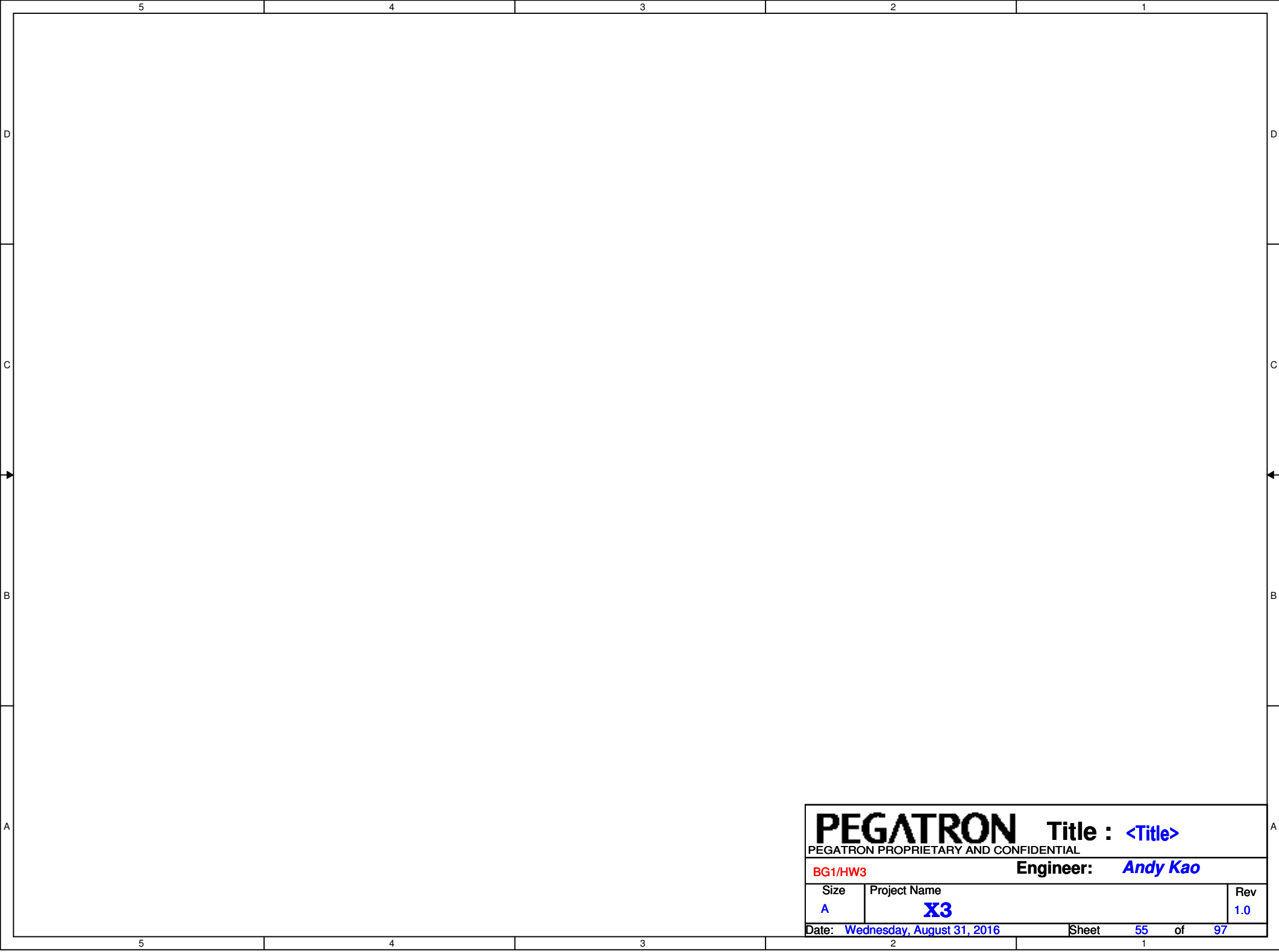
+3V_WLAN_WP1 bypass capacitor:
Place 0.1uF near pin 2,4
Place 10uF near +3V_WLAN_WP1 source side.



+3V_WLAN_WP1 bypass capacitor:
Place 0.1uF near pin 72,74.
Place 10uF near +3V_WLAN_WP1 source side.



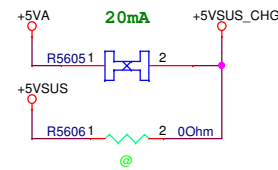
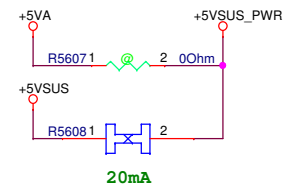
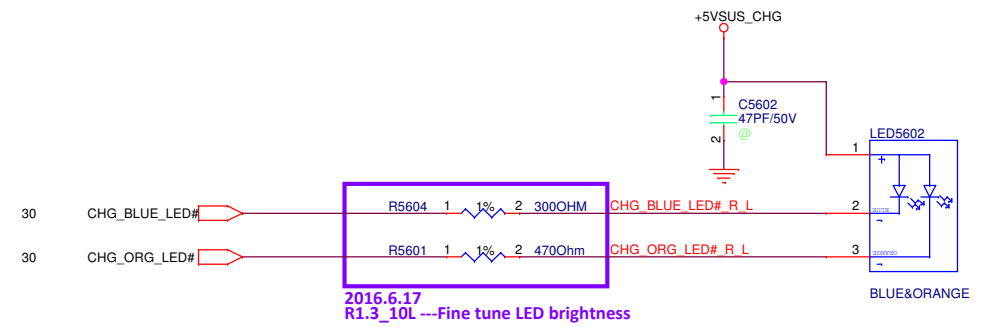
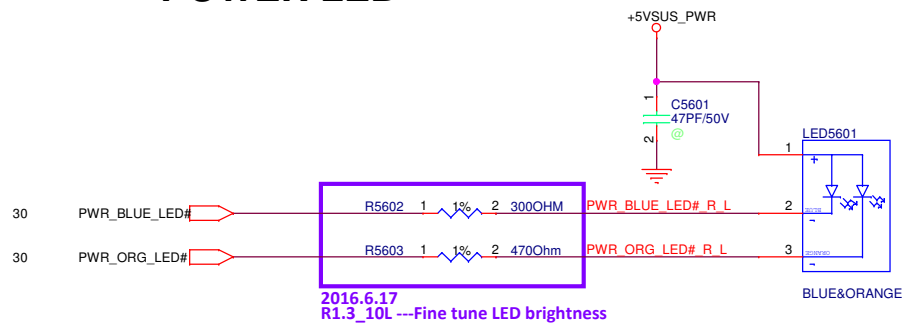
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PEGATRON										Title : USB HUB																																																																																																								
PEGATRON PROPRIETARY AND CONFIDENTIAL																																																																																																																		
<OrgName>										Engineer: Andy Kao																																																																																																								
Size		Project Name											Rev																																																																																																					
A		X3											1.0																																																																																																					
Date: Wednesday, August 31, 2016										Sheet 54 of 97																																																																																																								
5					4					3					2					1																																																																																														



PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size <i>A</i>	Project Name X3	Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>55</i> of <i>97</i>

POWER LED

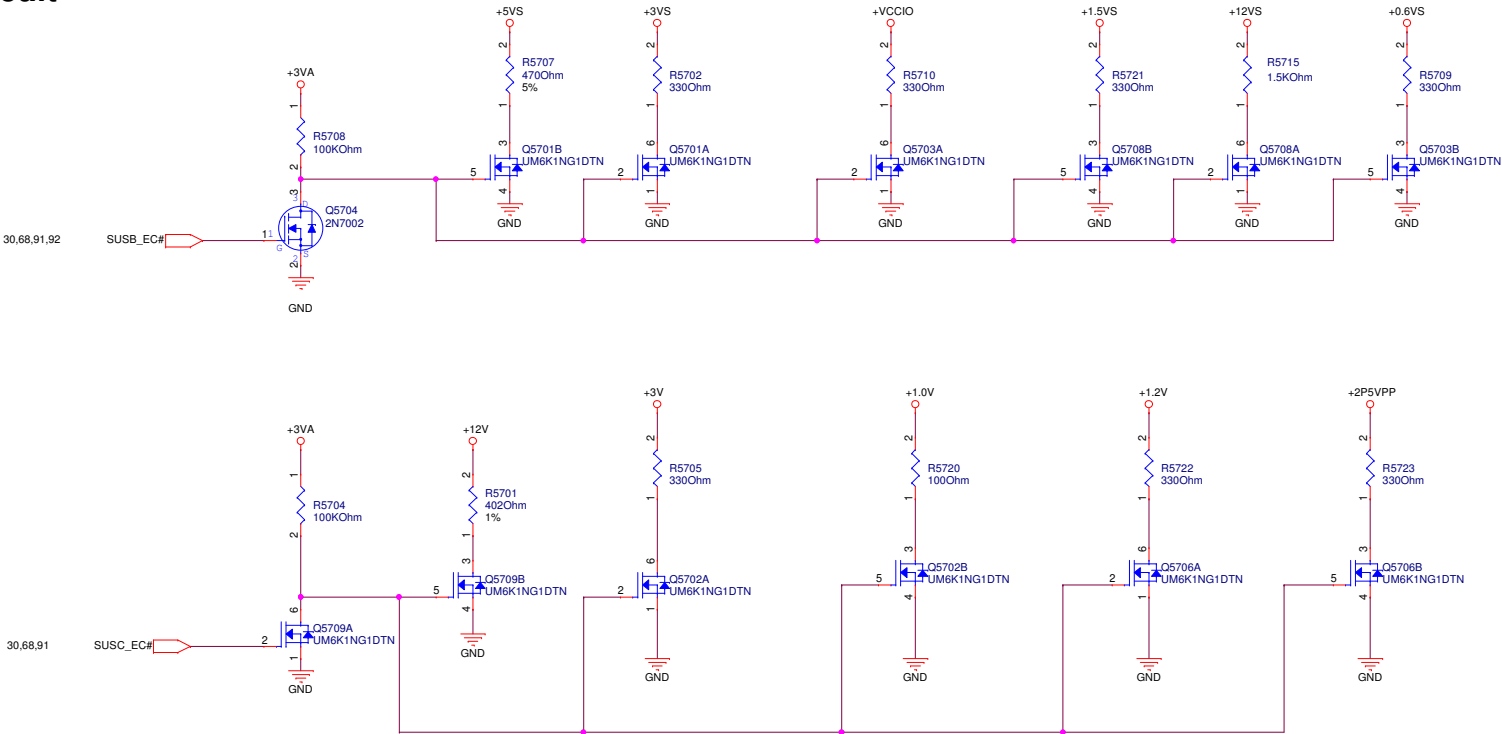
Charger LED

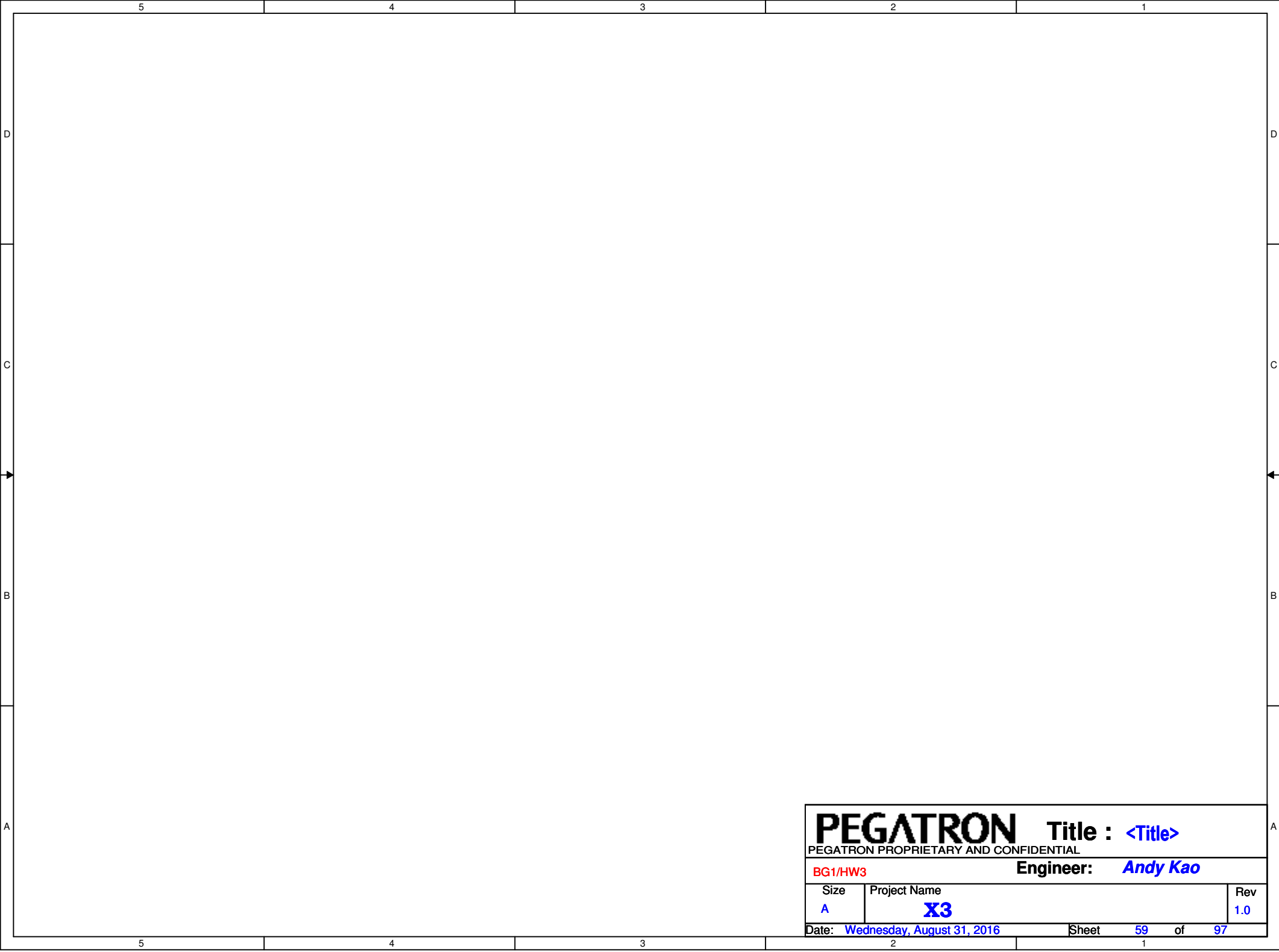


<Variant Name>

PEGATRON		Title : LED_Indicator	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Andy Kao	
Size B	Project Name X3		Rev 1.0
Date: Wednesday, August 31, 2016		Sheet	56 of 97

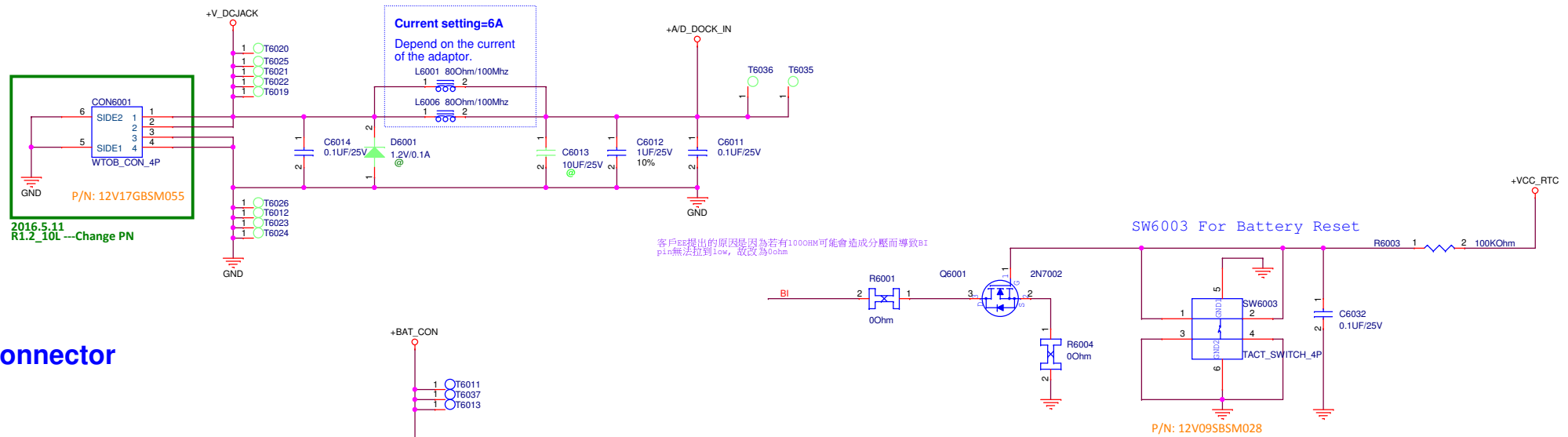
Discharge Circuit



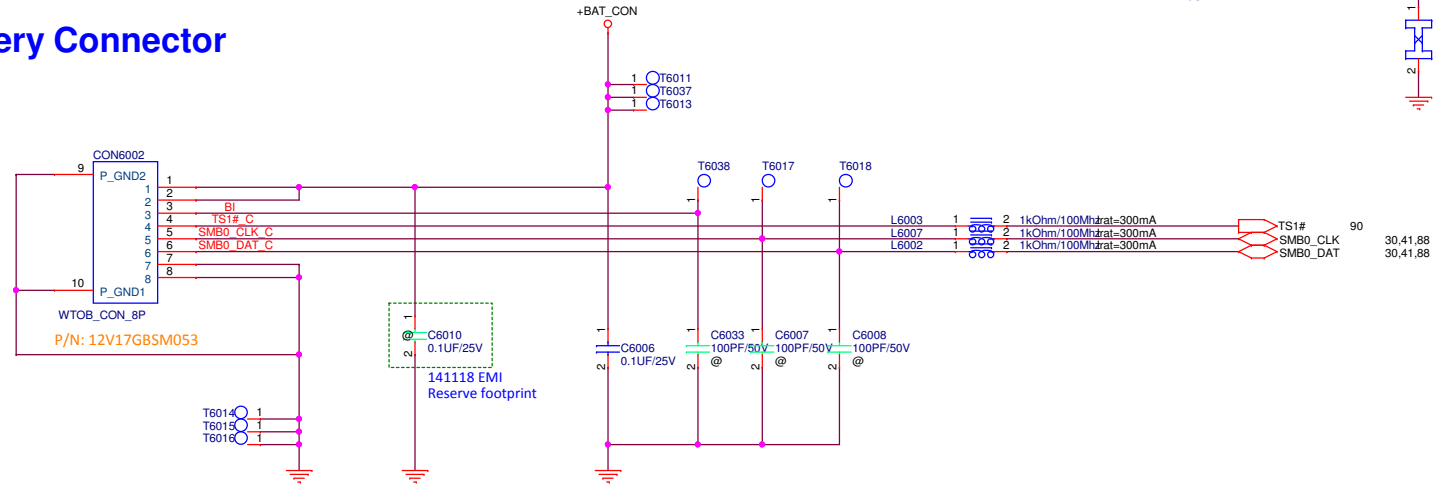


PEGATRON		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size <i>A</i>	Project Name X3		Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>59</i> of <i>97</i>	

DC Jack WtoB CONN



Battery Connector

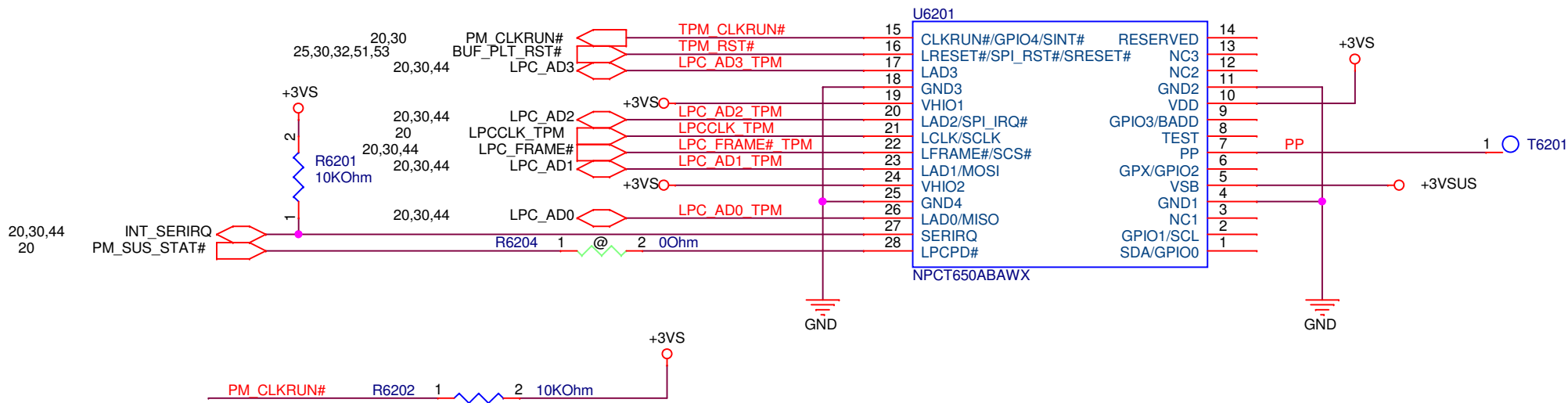
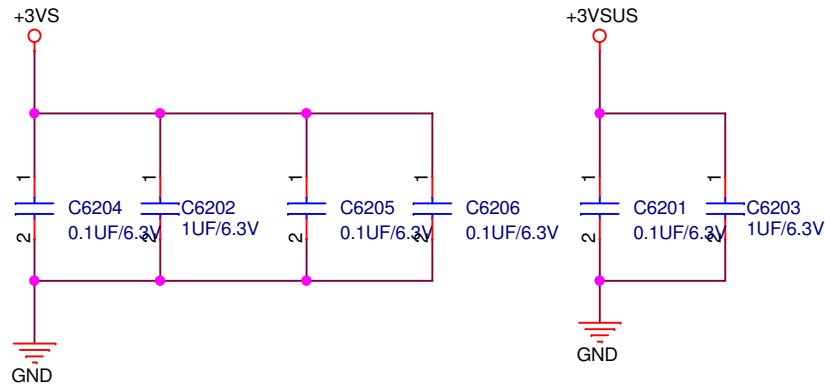


PEGATRON Title : <Title>

BG1/HW3 **Engineer:** *Andy Kao*

Size A	Project Name X3	Rev 1.0
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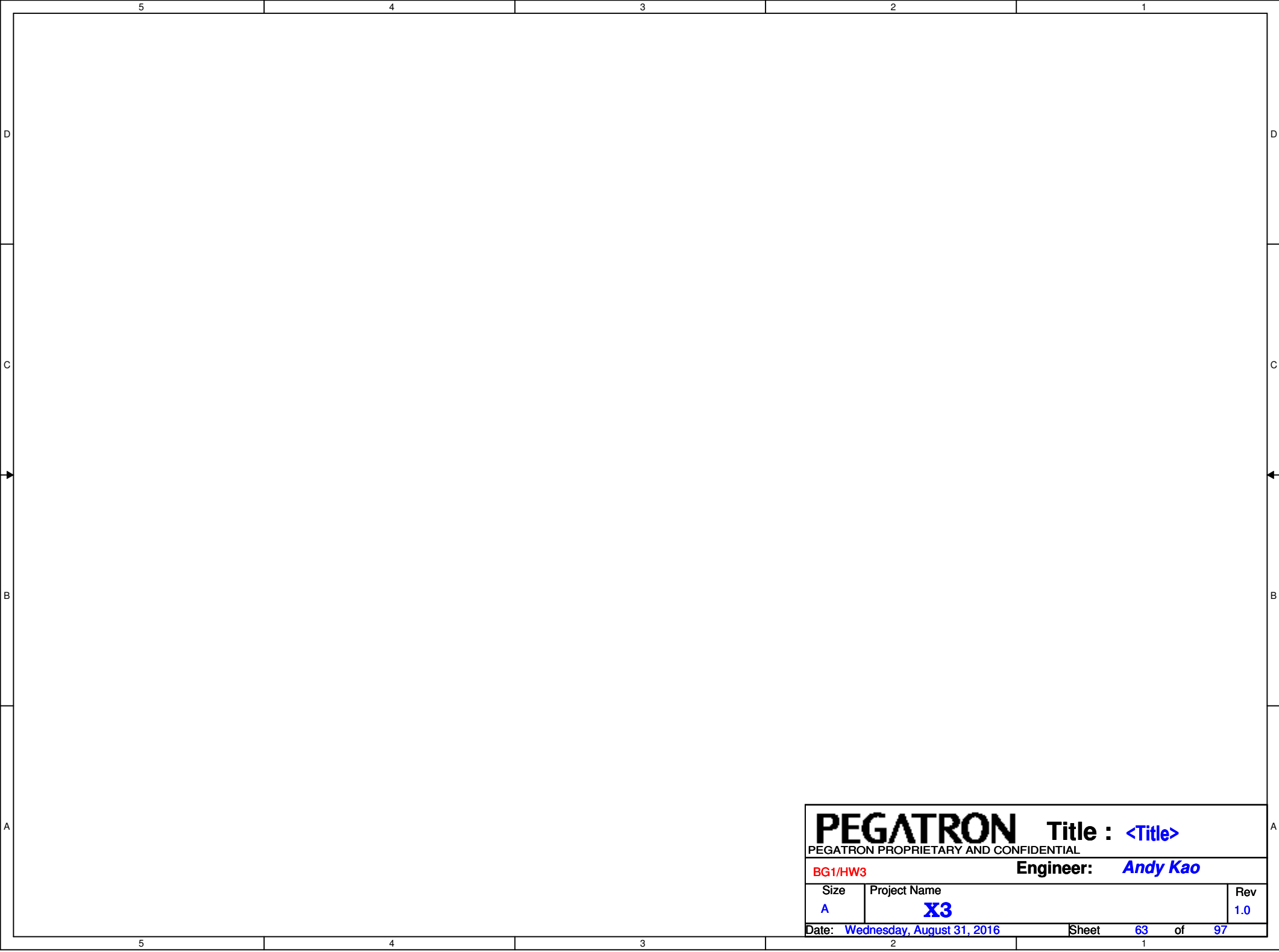
Date: Wednesday, August 31, 2016	Sheet 61 of 97
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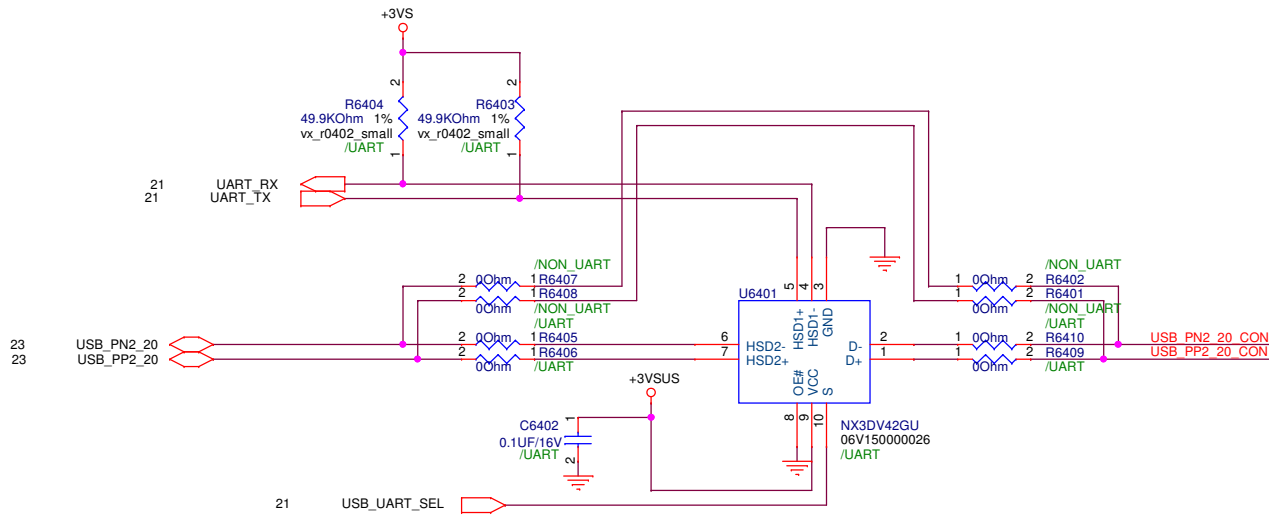
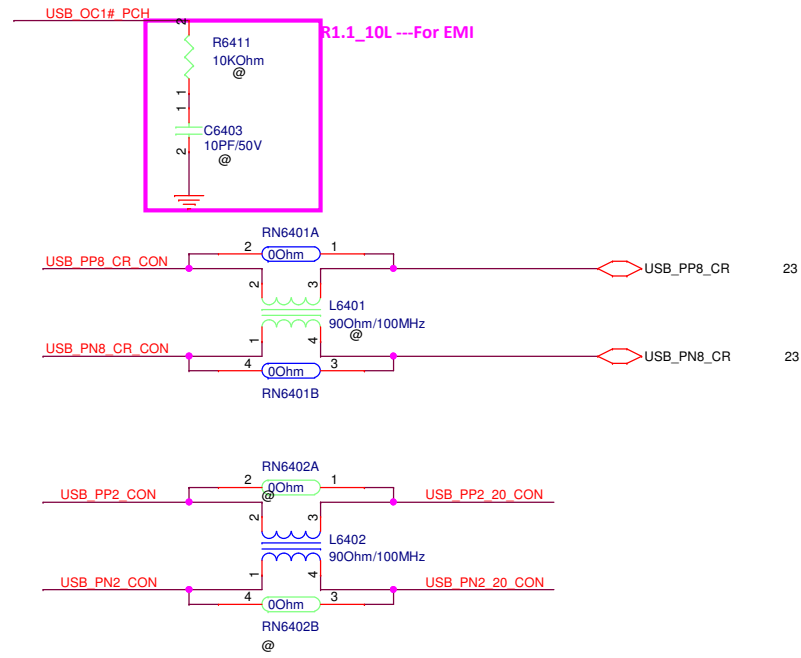
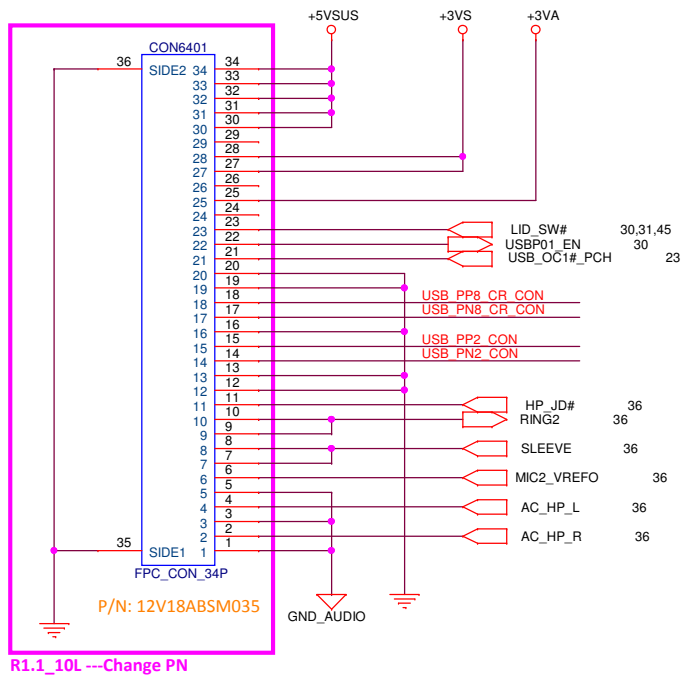
Vendor Suggest Pull High Resistor Need To Close To TPM
PM_CLKRUN#, INT_SERIRQ Need To Pull 10Kohm To+3VS at Chipset Side

<Variant Name>

PEGATRON		Title : TPM CONN	
BG1/HW3		Engineer: Andy Kao	
Size Custom	Project Name X3		Rev 1.0
Date: Wednesday, August 31, 2016		Sheet 62 of 97	



PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size <i>A</i>	Project Name X3	Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>63</i> of <i>97</i>

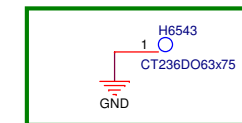
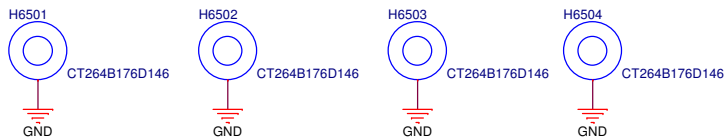


<Variant Name>		
PEGATRON Title : IO CON. PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3 Engineer: Andy Kao		
Size B	Project Name X3	Rev 1.0
Date: Wednesday, August 31, 2016 Sheet 64 of 97		

CPU NUT

6*2.5mm*1

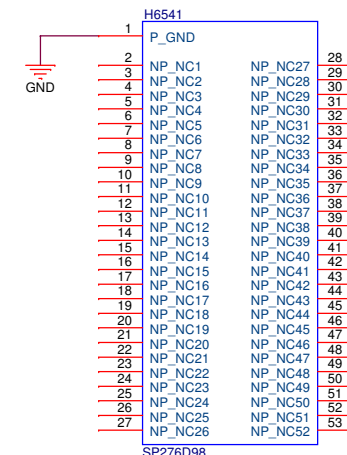
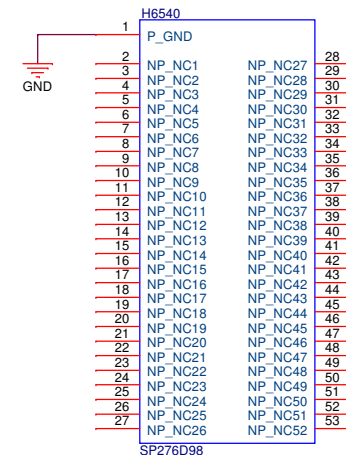
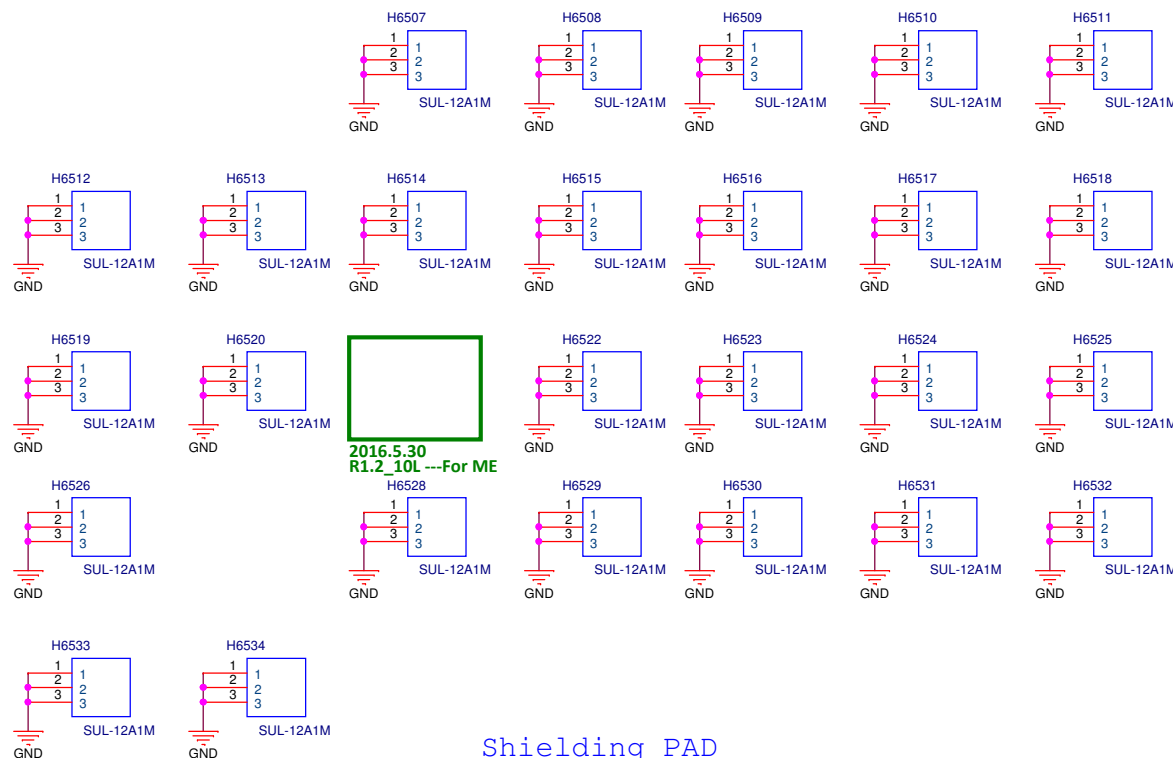
6*3.1mm*1



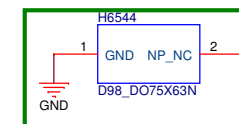
2016.6.6 R1.2_10L ---For ME

CLIP

Thermal screw*2

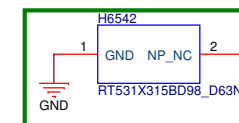


14*8mm*1



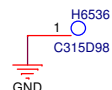
2016.6.6 R1.2_10L ---For ME

13.5*8mm*1

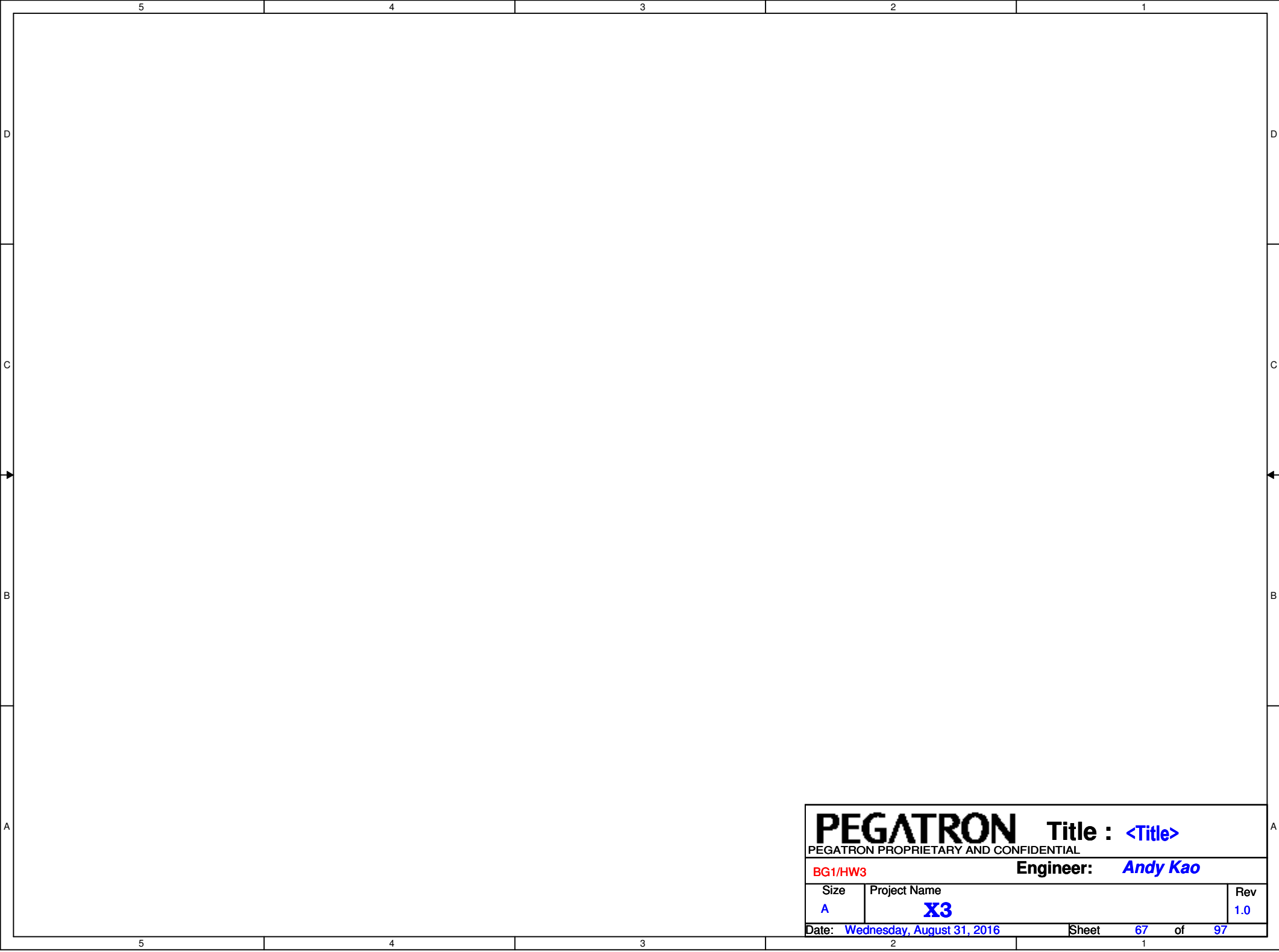


2016.6.6 R1.2_10L ---For ME

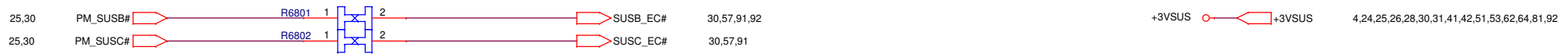
Shielding PAD



PEGATRON		Title : NUT,Screw Hole	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Andy Kao	
Size B	Project Name X3		Rev 1.0
Date: Wednesday, August 31, 2016		Sheet 65 of 97	

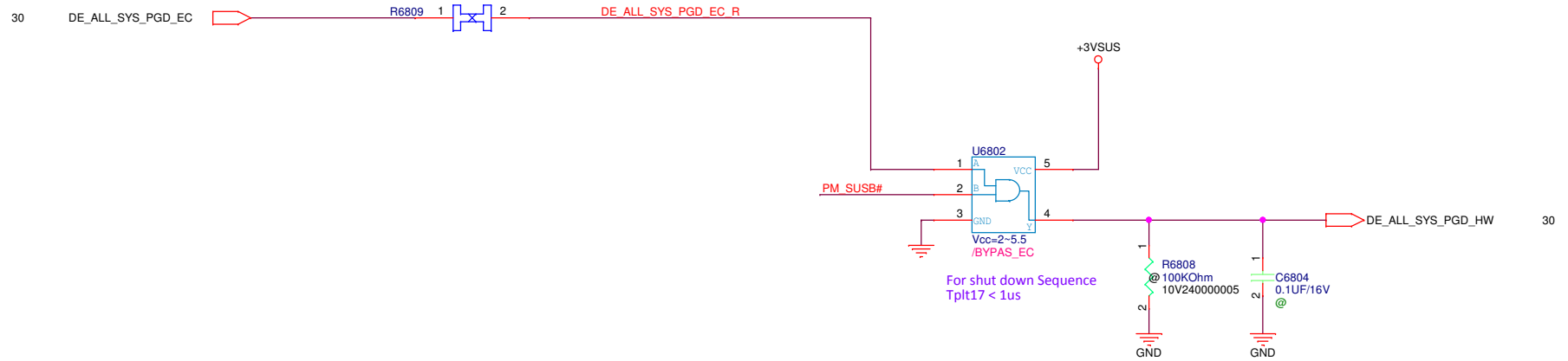


PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size <i>A</i>	Project Name X3	Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>67</i> of <i>97</i>

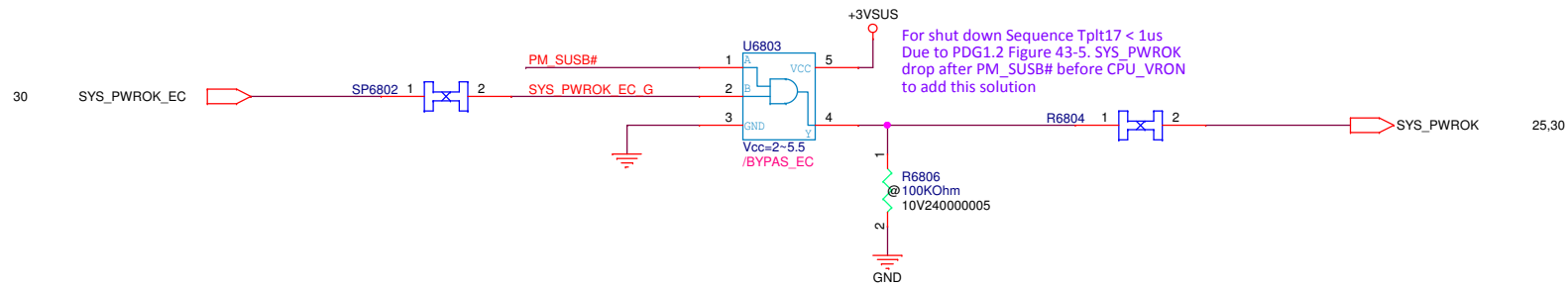


For Intel power sequence requestment
ALL_SYS_PWRGD to Delay_ALL_SYS_PGD >2ms

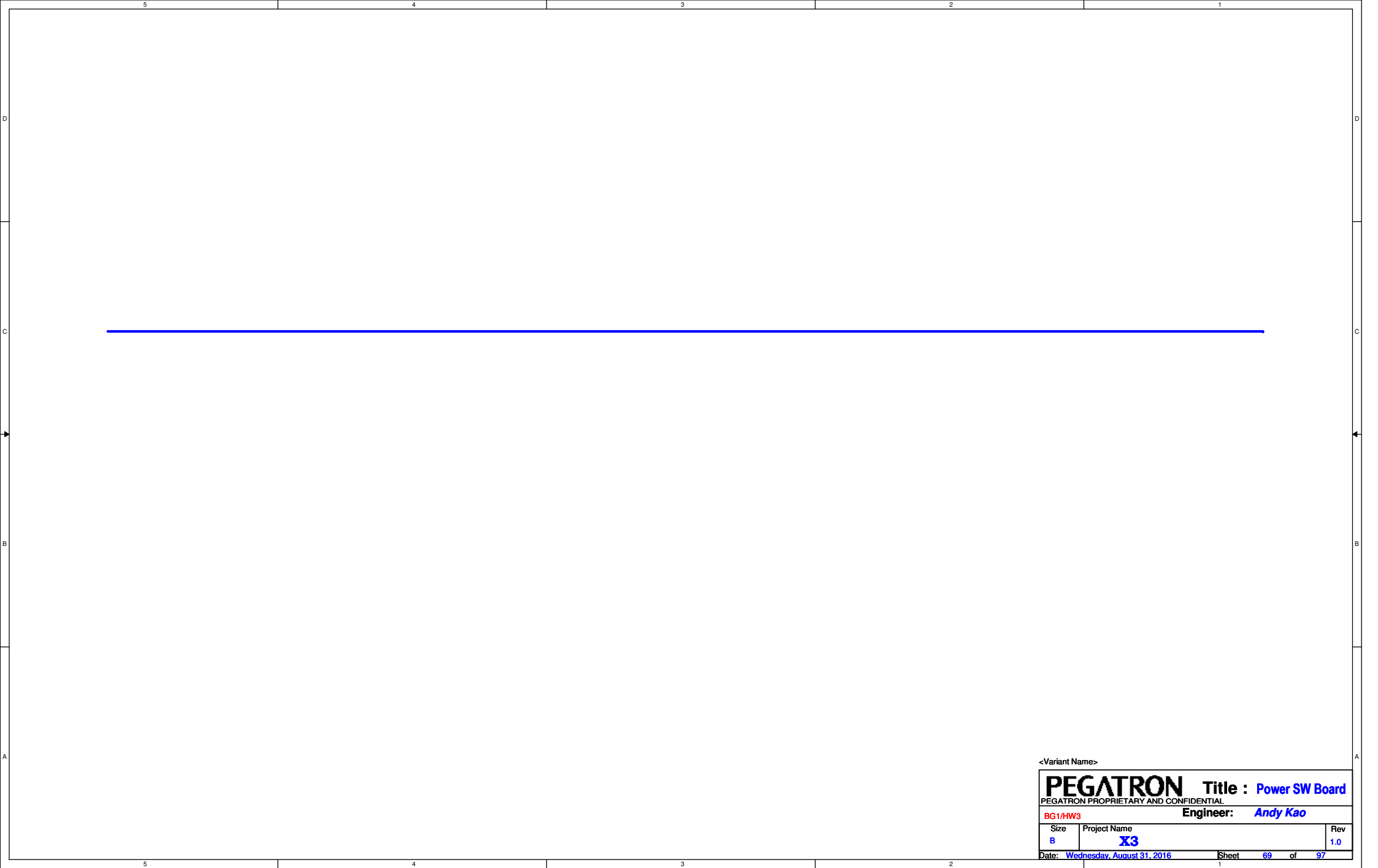
Delay By EC(2ms+ EC processing time (3ms~33ms))



For shut down Sequence
Tplt17 < 1us

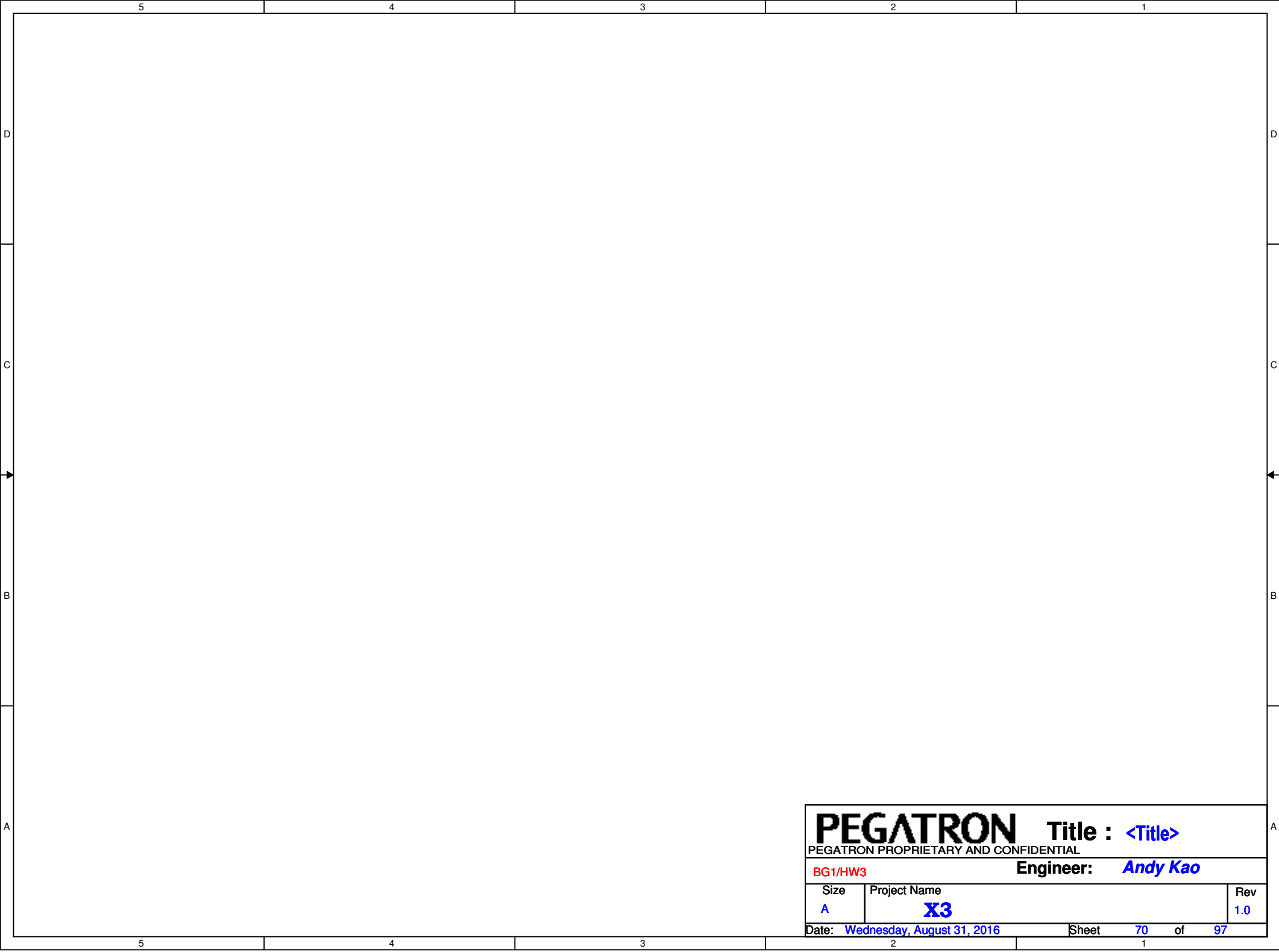


For shut down Sequence Tplt17 < 1us
Due to PDG1.2 Figure 43-5. SYS_PWROK
drop after PM_SUSB# before CPU_VRON
to add this solution

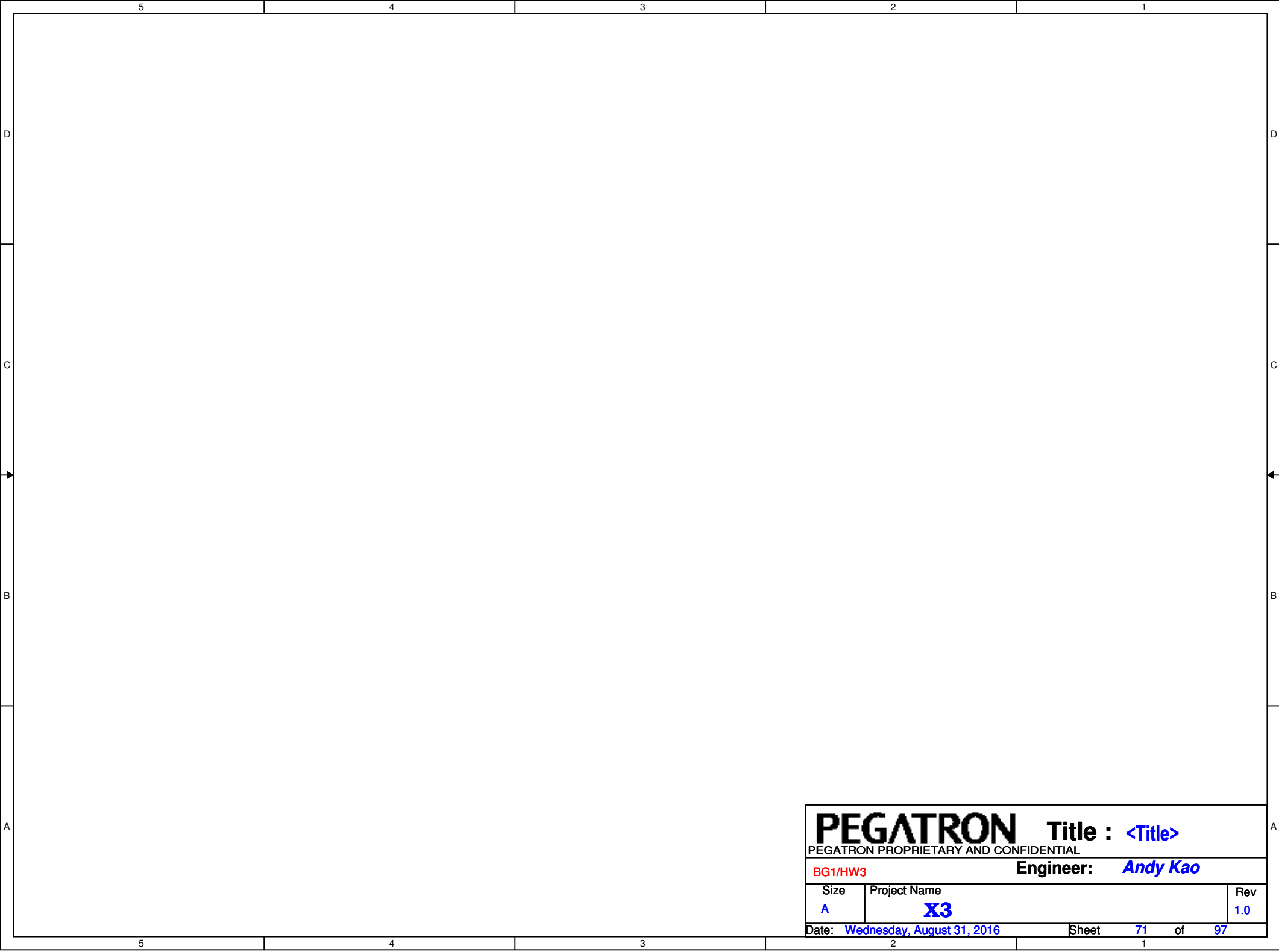


<Variant Name>

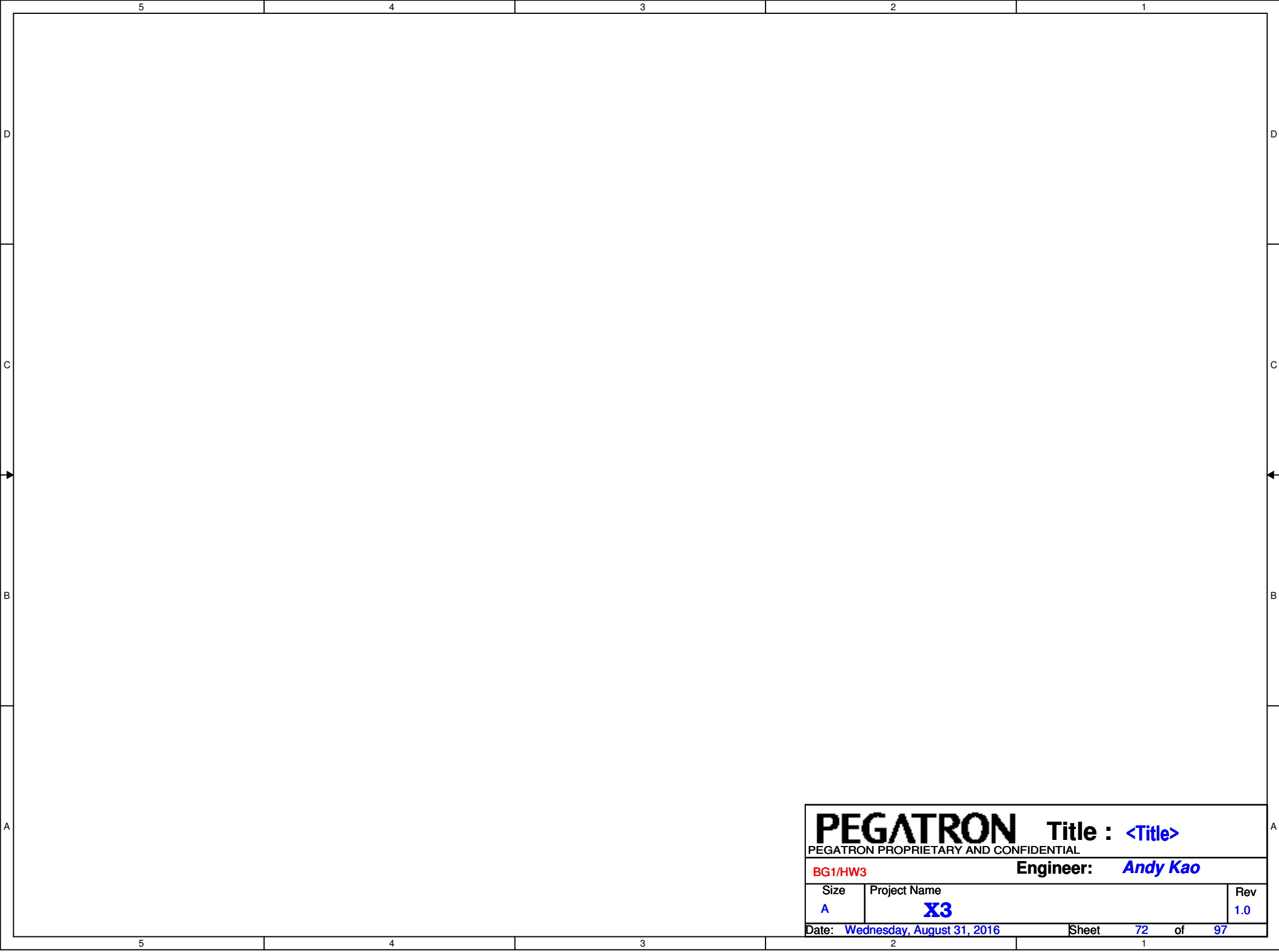
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Andy Kao	
Size	Project Name		Rev
B	X3		1.0
Date: Wednesday, August 31, 2016		Sheet	69 of 97



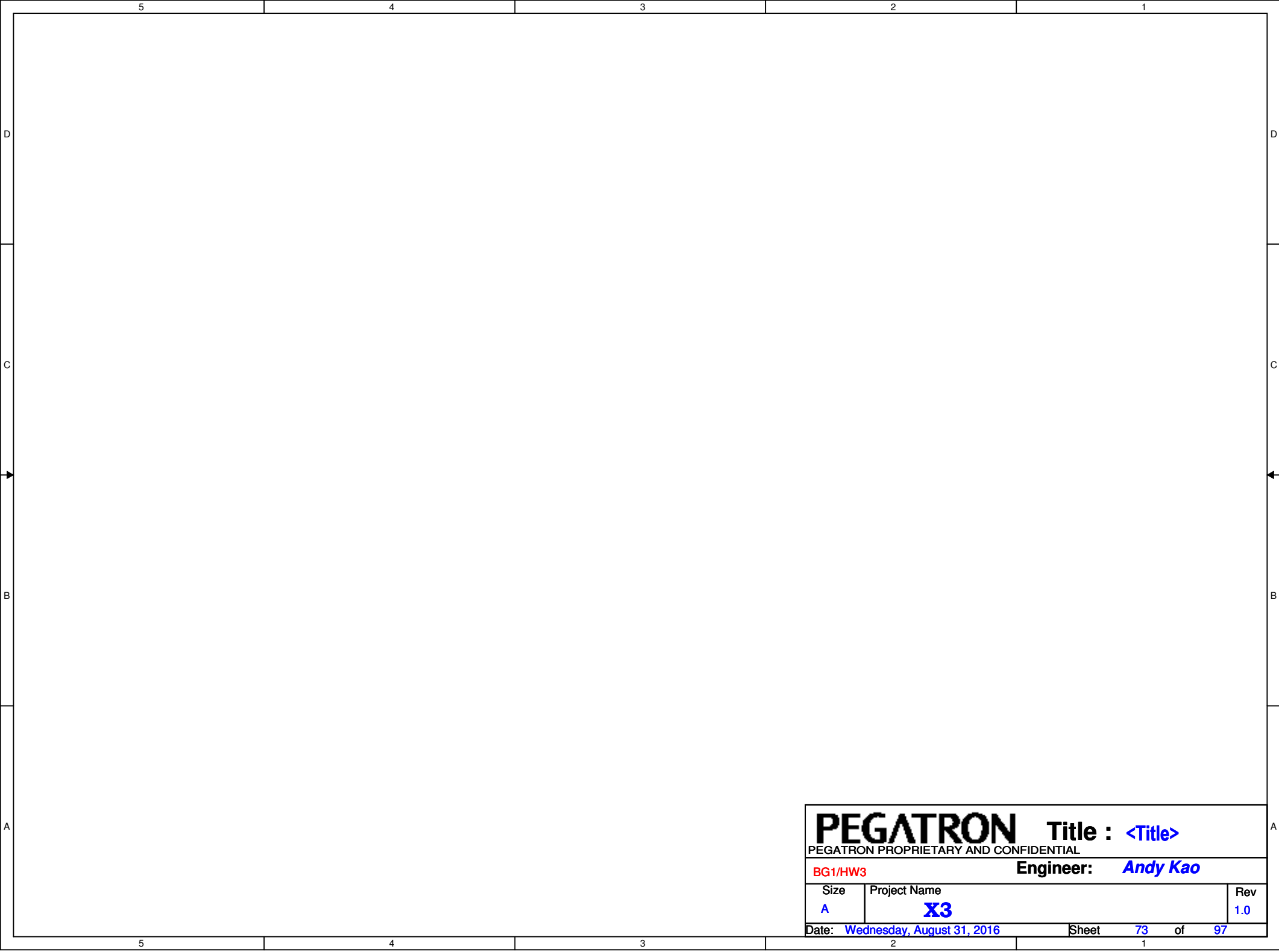
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size <i>A</i>	Project Name X3		Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>70</i> of <i>97</i>	



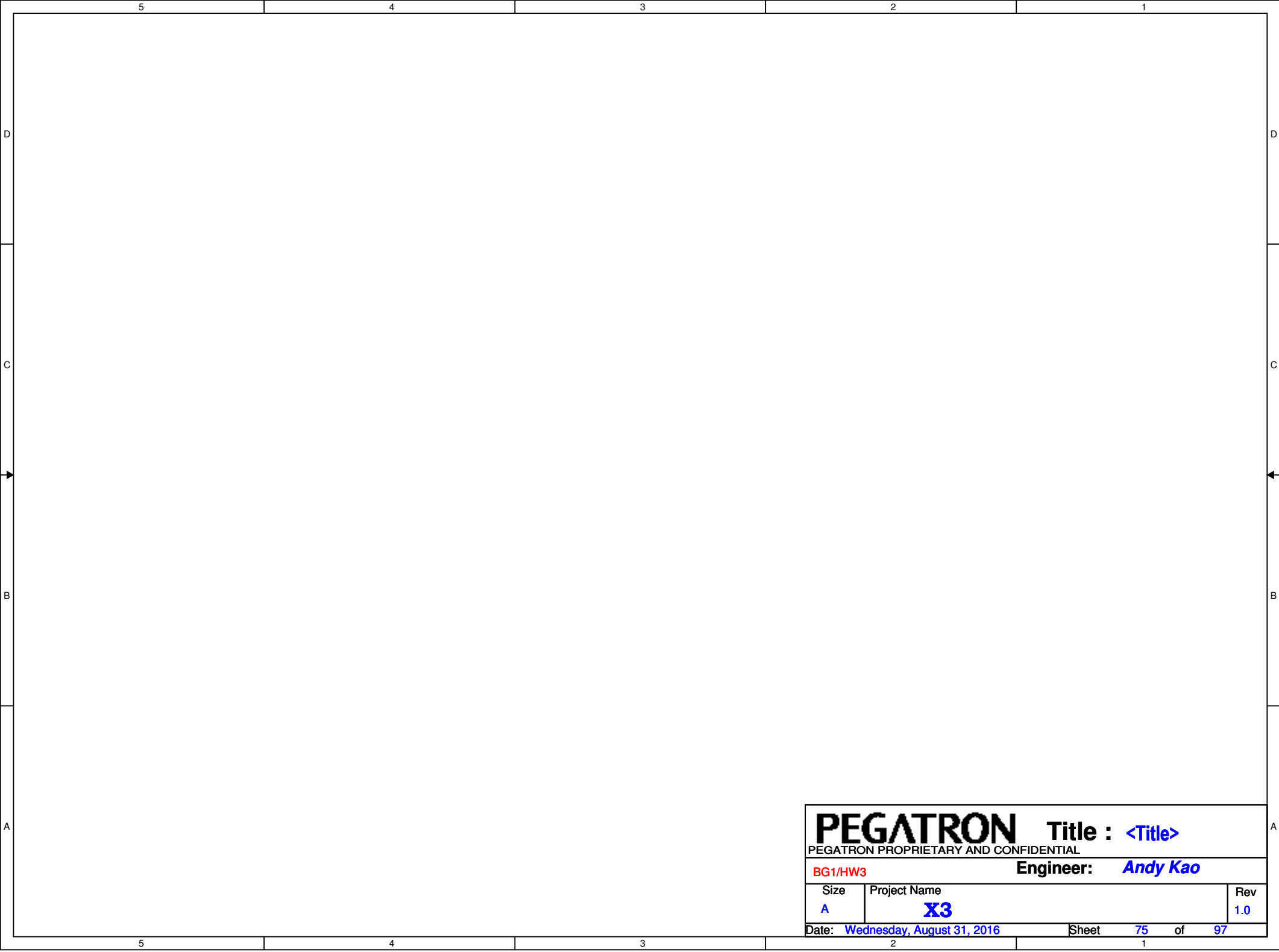
PEGATRON		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size <i>A</i>	Project Name X3		Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>71</i> of <i>97</i>	



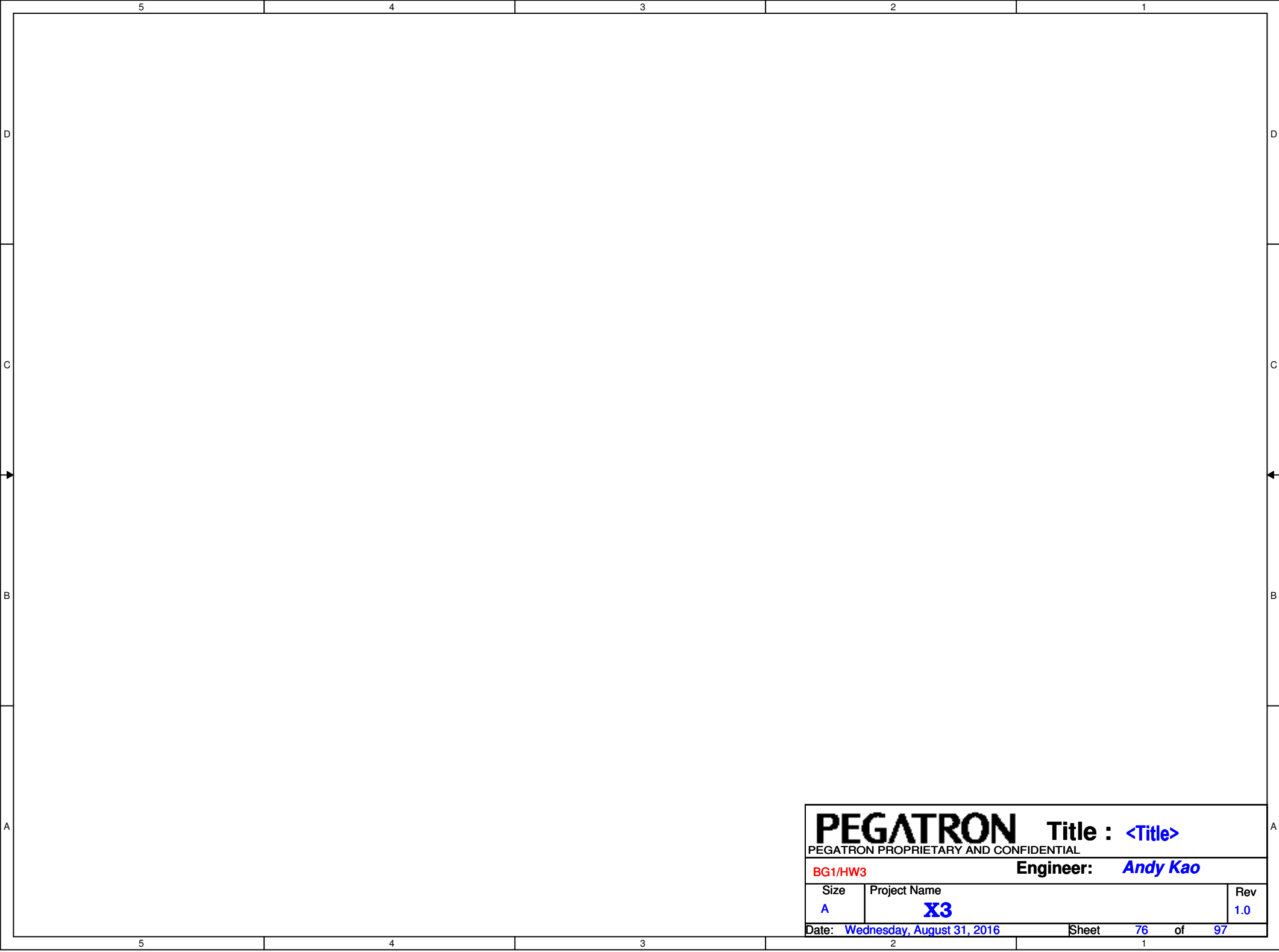
PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size <i>A</i>	Project Name X3	Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>72</i> of <i>97</i>



PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size A	Project Name X3	Rev 1.0
Date: Wednesday, August 31, 2016		Sheet 73 of 97



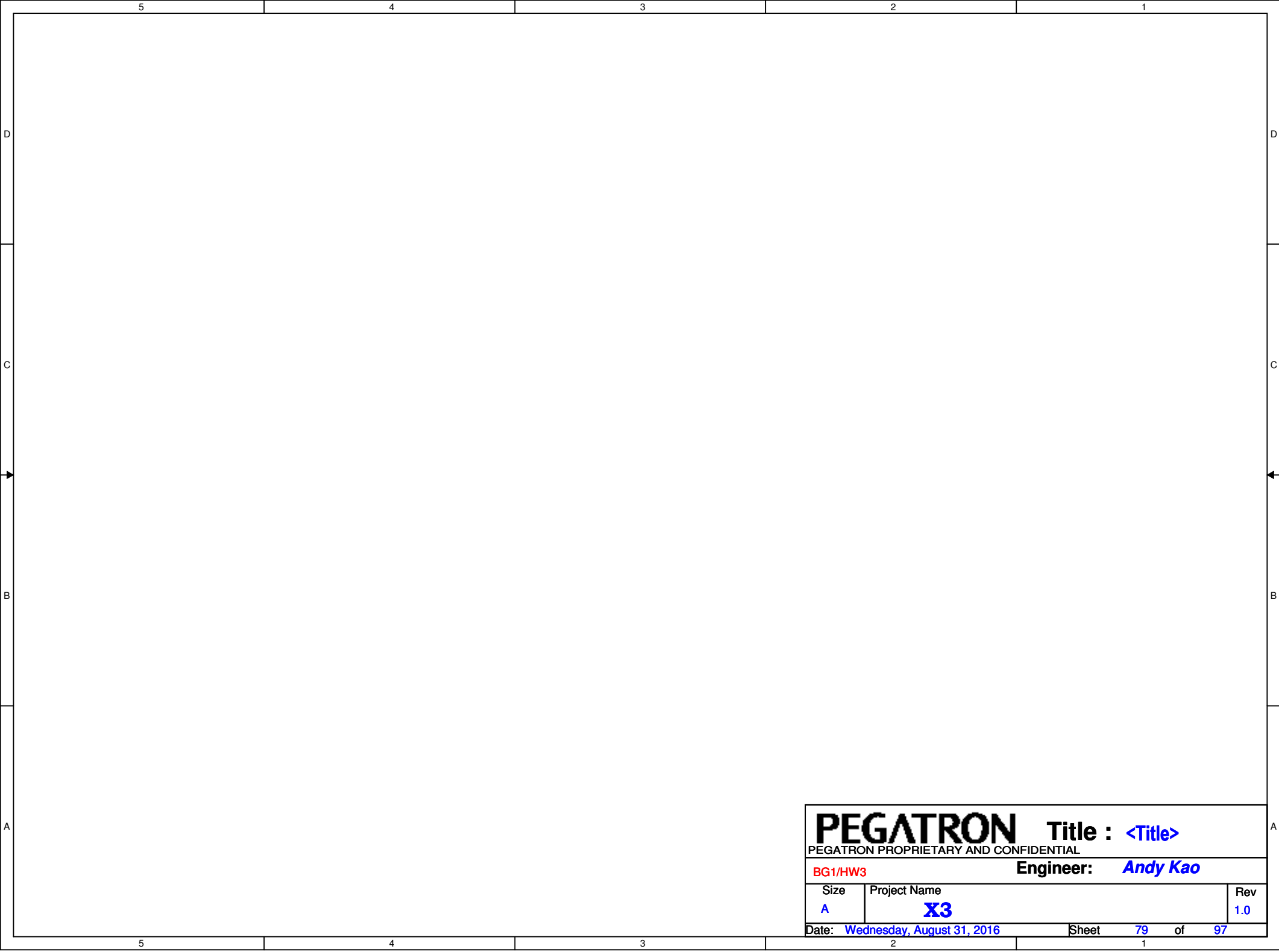
PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size A	Project Name X3	Rev 1.0
Date: Wednesday, August 31, 2016		Sheet 75 of 97



PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size A	Project Name X3	Rev 1.0
Date: Wednesday, August 31, 2016		Sheet 76 of 97

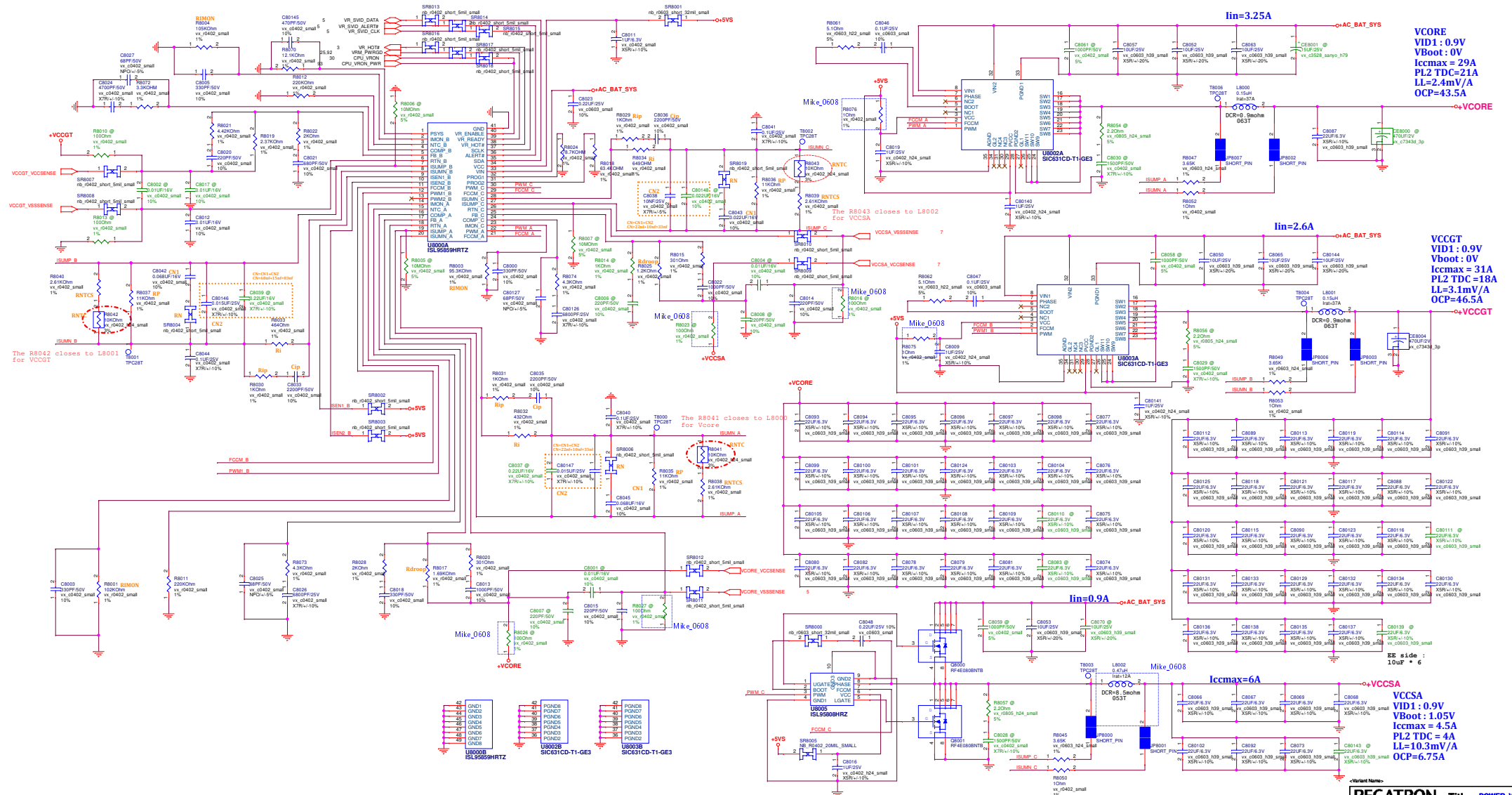
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										<table><tr><td colspan="10">PEGATRON</td><td colspan="5">Title : <Title></td></tr><tr><td colspan="15">PEGATRON PROPRIETARY AND CONFIDENTIAL</td></tr><tr><td colspan="10">BG1/HW3</td><td colspan="5">Engineer: Andy Kao</td></tr><tr><td colspan="2">Size</td><td colspan="10">Project Name</td><td colspan="3">Rev</td></tr><tr><td colspan="2">A</td><td colspan="10">X3</td><td colspan="3">1.0</td></tr><tr><td colspan="10">Date: Wednesday, August 31, 2016</td><td colspan="5">Sheet 77 of 97</td></tr></table>															PEGATRON										Title : <Title>					PEGATRON PROPRIETARY AND CONFIDENTIAL															BG1/HW3										Engineer: Andy Kao					Size		Project Name										Rev			A		X3										1.0			Date: Wednesday, August 31, 2016										Sheet 77 of 97				
PEGATRON										Title : <Title>																																																																																																								
PEGATRON PROPRIETARY AND CONFIDENTIAL																																																																																																																		
BG1/HW3										Engineer: Andy Kao																																																																																																								
Size		Project Name										Rev																																																																																																						
A		X3										1.0																																																																																																						
Date: Wednesday, August 31, 2016										Sheet 77 of 97																																																																																																								
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PEGATRON										Title : <Title>																																																																																																								
PEGATRON PROPRIETARY AND CONFIDENTIAL																																																																																																																		
BG1/HW3										Engineer: Andy Kao																																																																																																								
Size		Project Name										Rev																																																																																																						
A		X3										1.0																																																																																																						
Date: Wednesday, August 31, 2016										Sheet 78 of 97																																																																																																								
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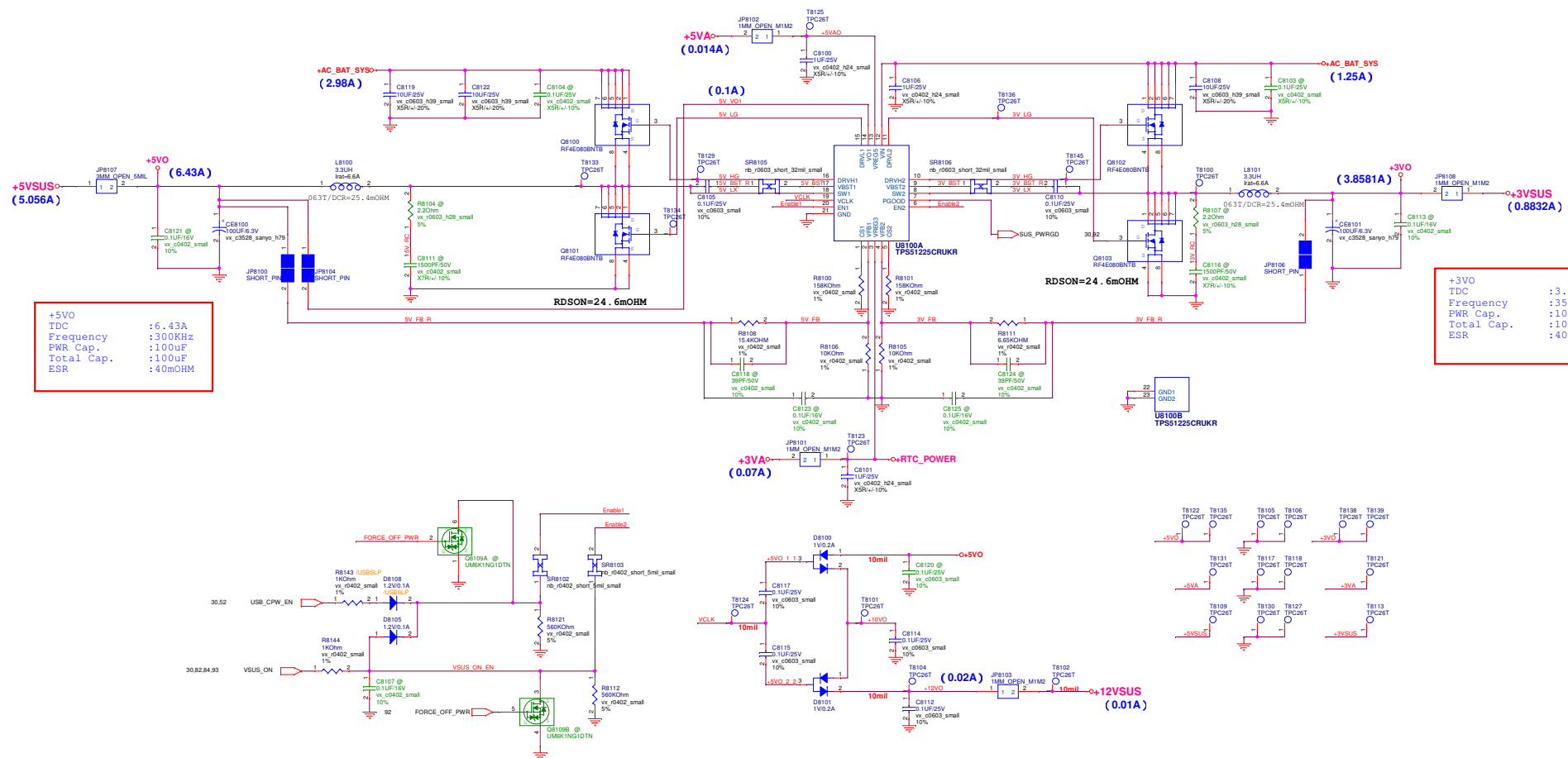


PEGATRON		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size <i>A</i>	Project Name X3		Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>79</i> of <i>97</i>	

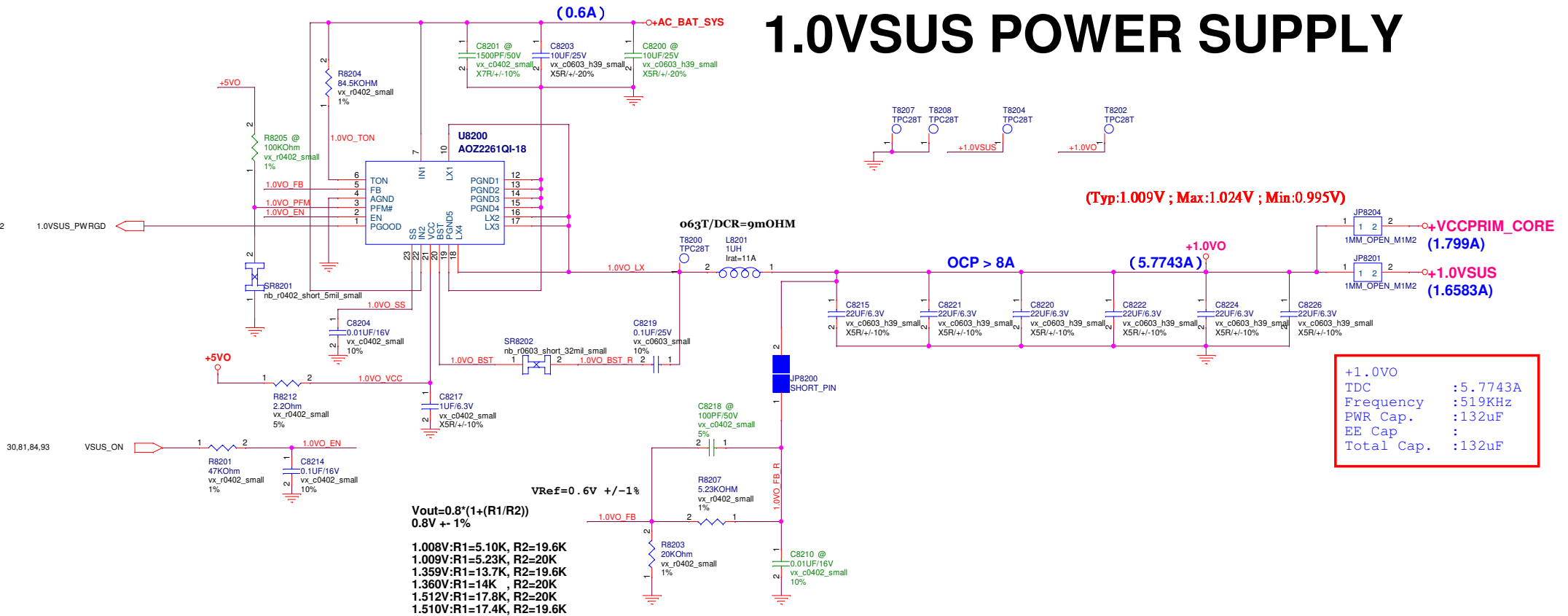
VCORE & VCCGT & VCCSA POWER SUPPLY



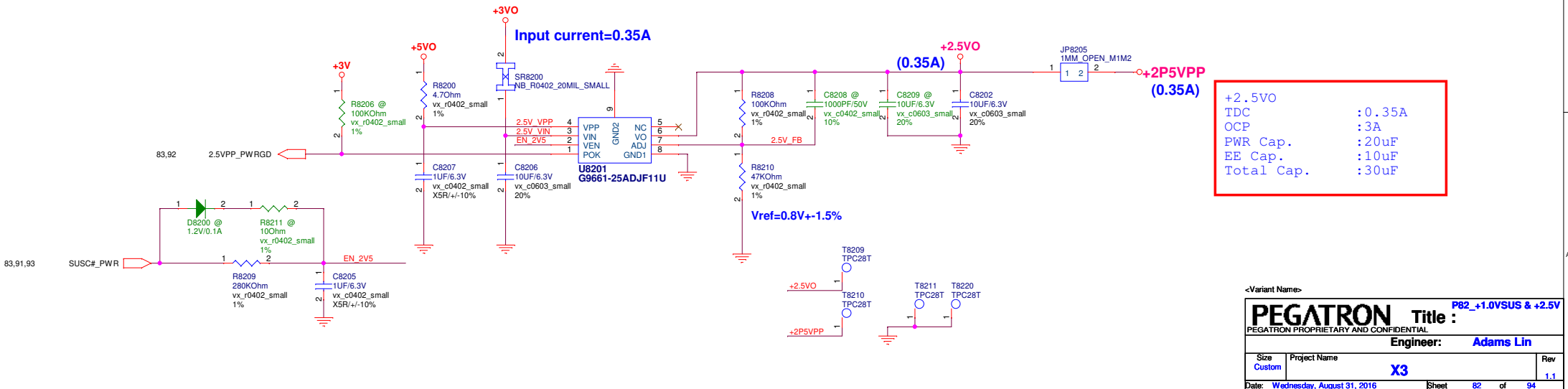
5V0 & 3V0 POWER SUPPLY



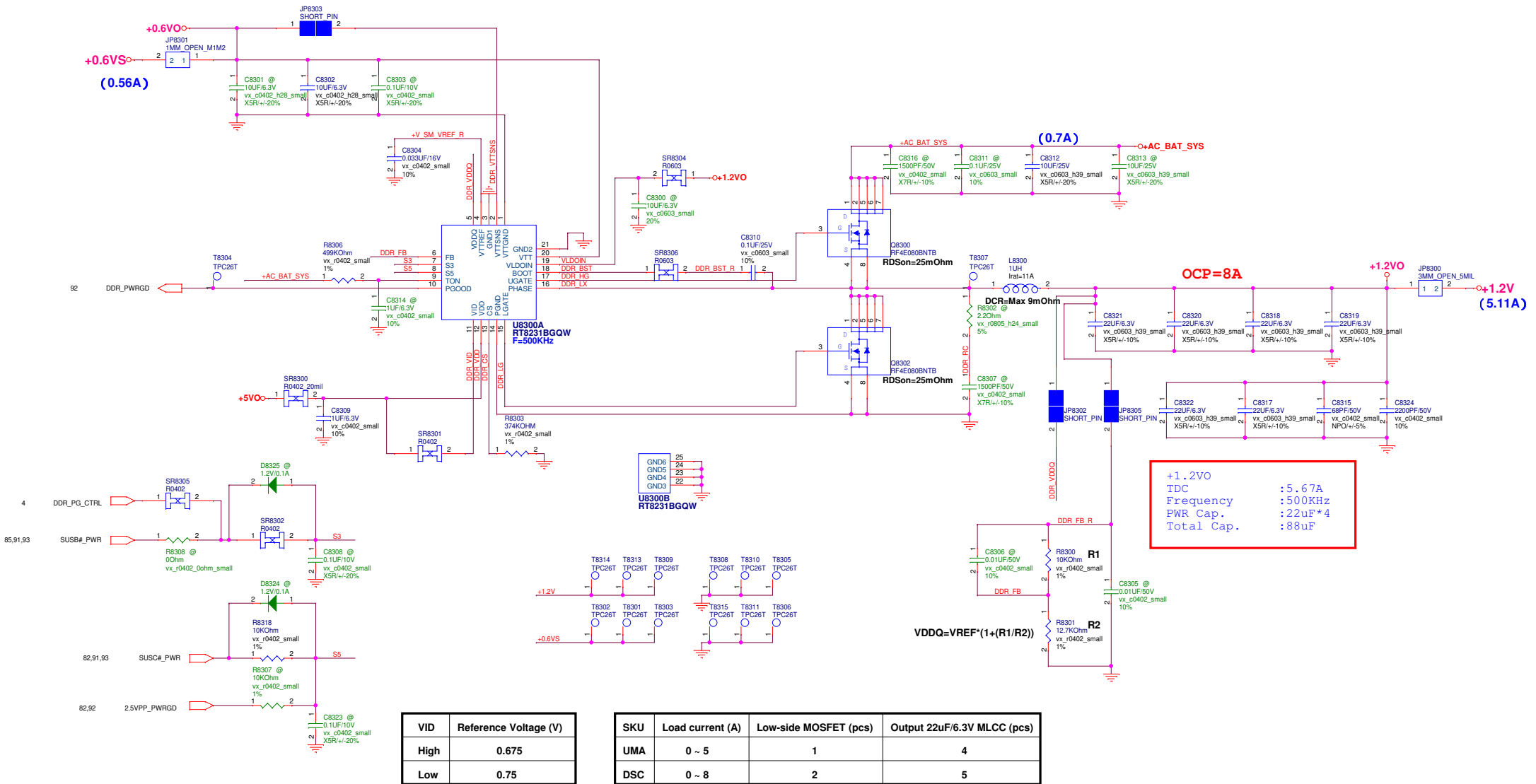
1.0VSUS POWER SUPPLY



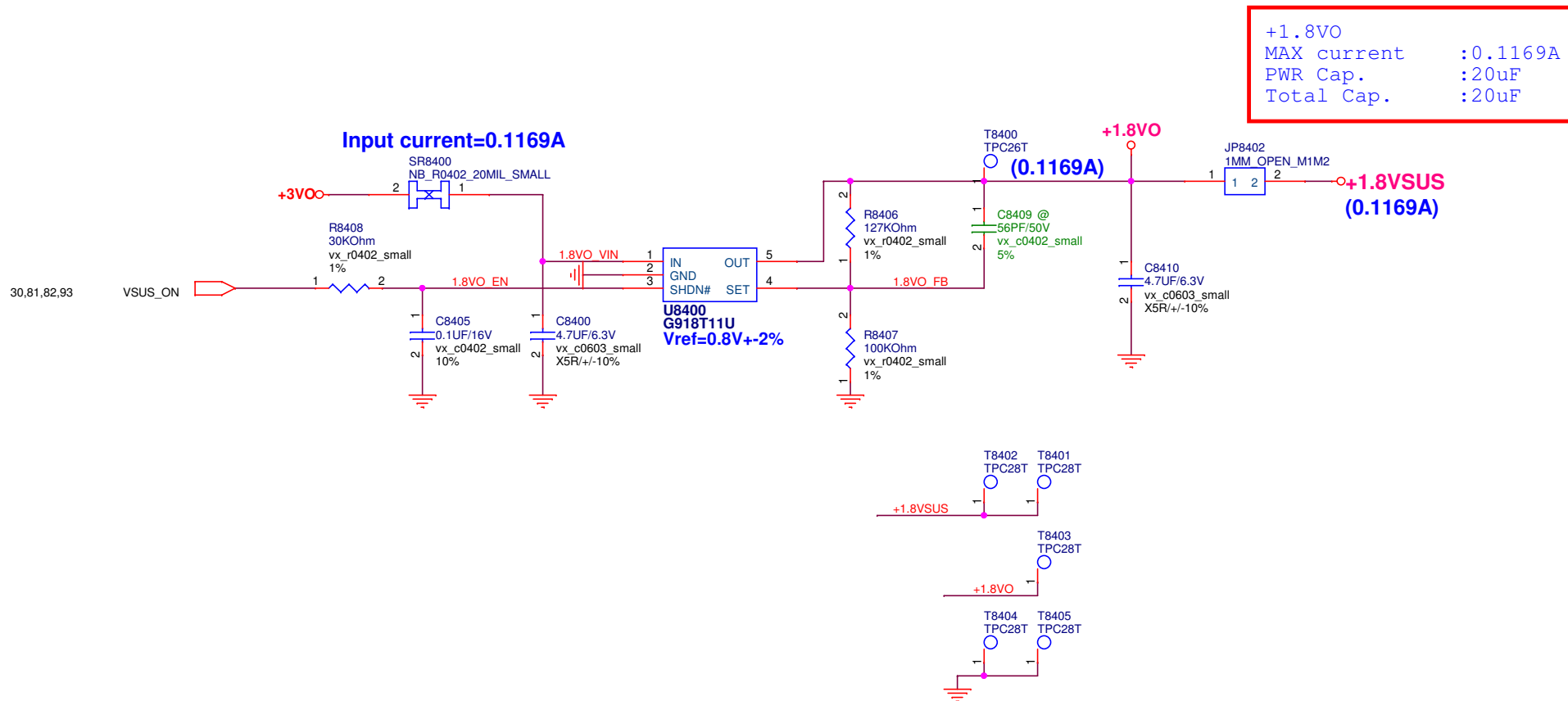
2.5V POWER SUPPLY



DDR & VTT POWER SUPPLY



1.8VSUS POWER SUPPLY



<Variant Name>

PEGATRON Title : POWER_+1.8VSUS

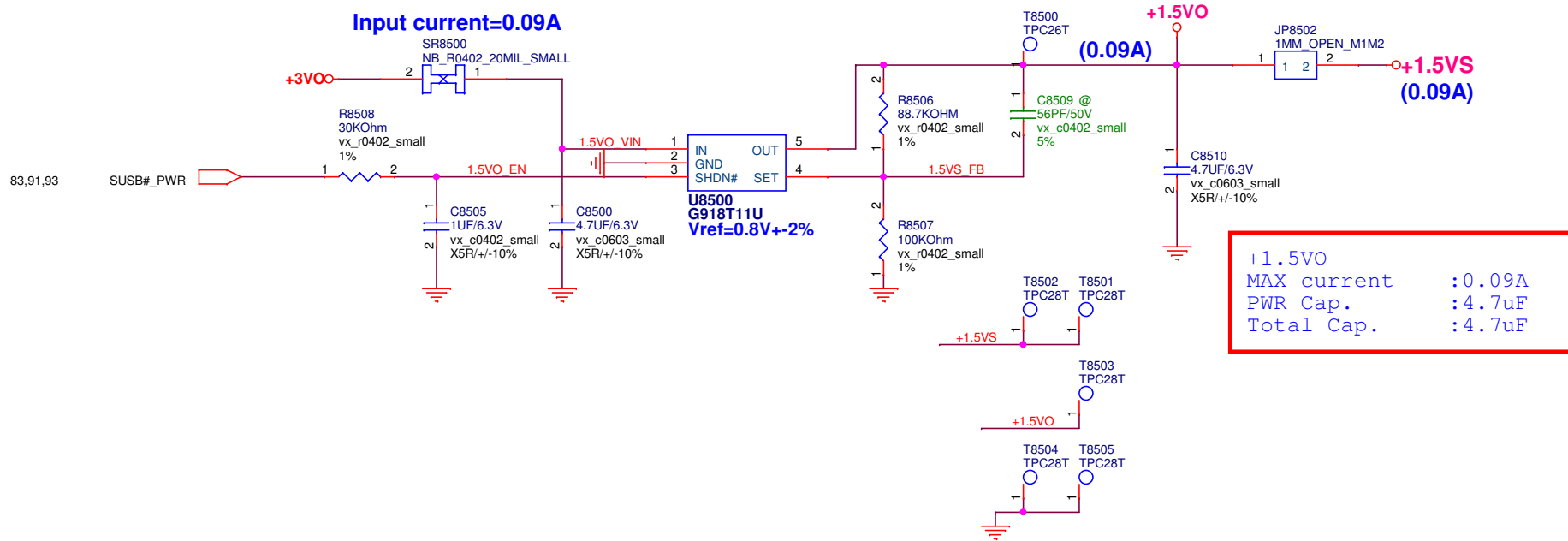
Engineer: Adams Lin

Size Custom	Project Name Y3	Rev
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Date: Wednesday, August 31, 2016

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1.5VS POWER SUPPLY



<Variant Name>

PEGATRON Title : POWER_+1.5VS

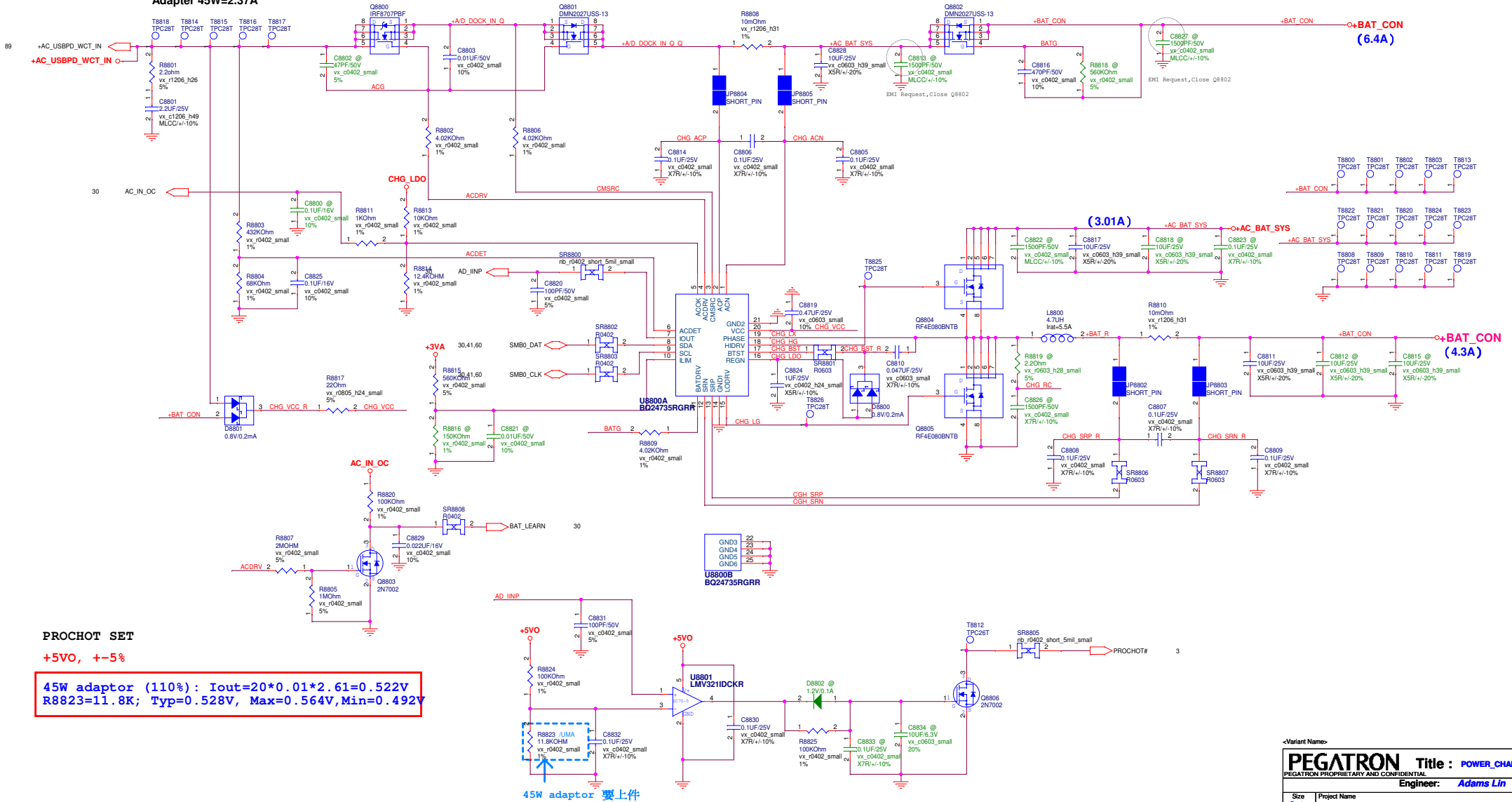
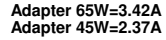
Engineer: Adams Lin

Size Custom	Project Name Y3	Rev
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Date: Wednesday, August 31, 2016

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BATTERY CHARGER



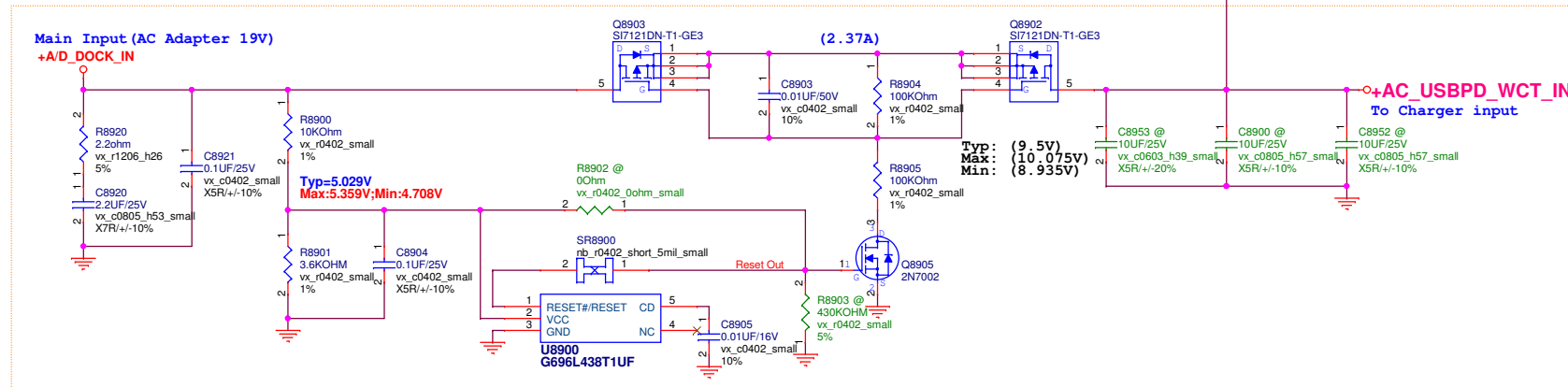
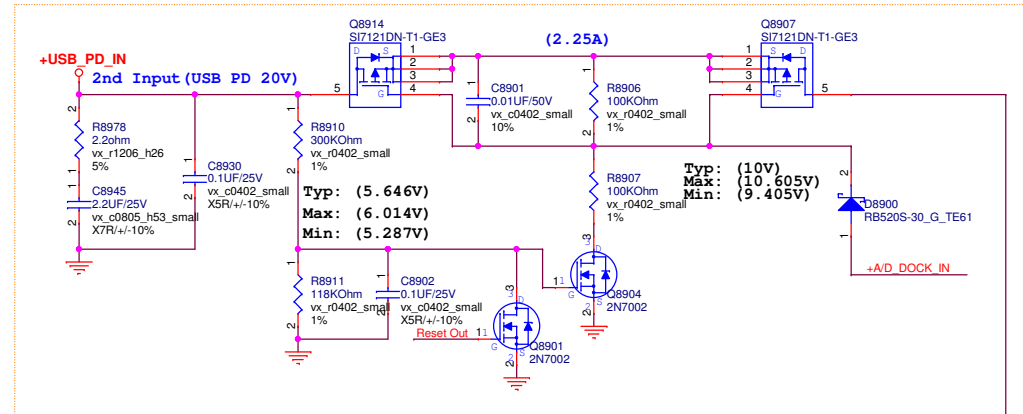
PROCHOT SET

+5V0, +−5%

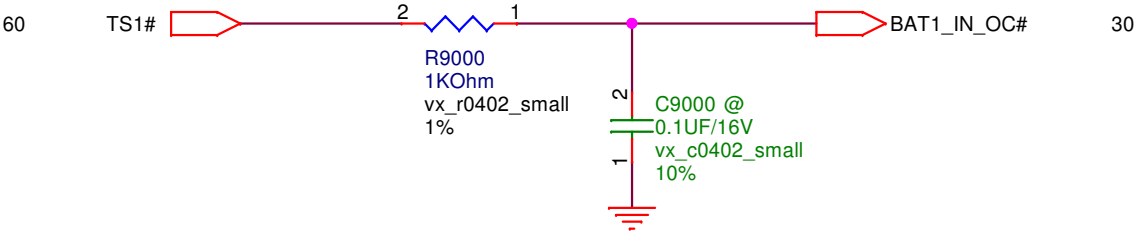
45W adaptor (110%): $I_{out}=20*0.01*2.61=0.522V$
R8823=11.8K; Typ=0.528V, Max=0.564V, Min=0.492V

45W adaptor 要上件

2 Input switch Circuit



BATTERY IN DETECT

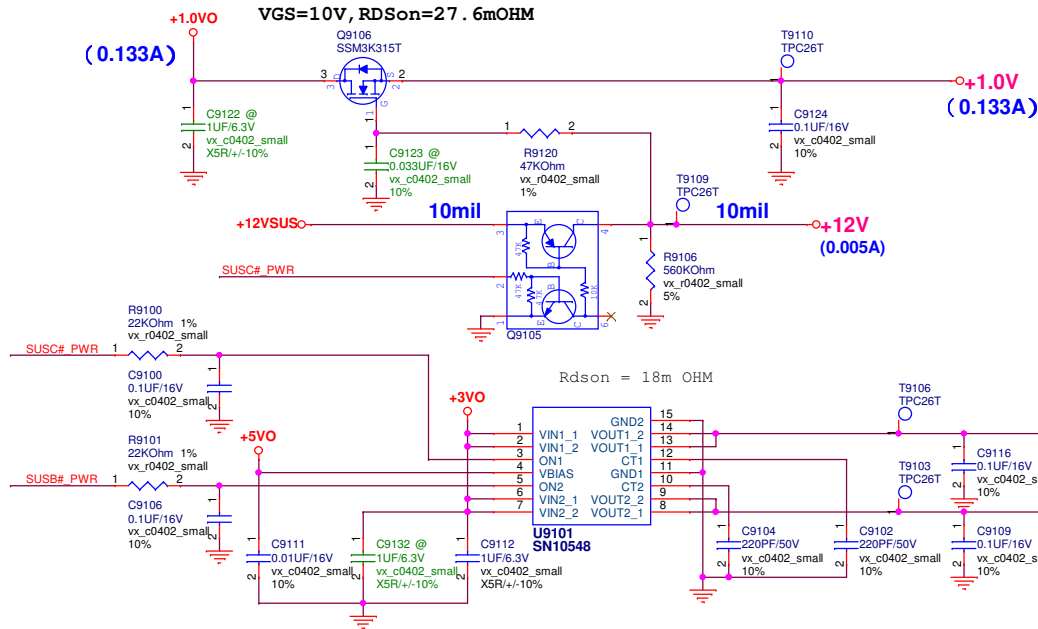


<Variant Name>

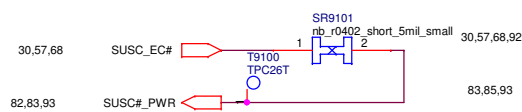
PEGATRON		Title : POWER_DETECT	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer: Adams Lin	
Size Custom	Project Name X3		Rev 1.1
Date:	Wednesday, August 31, 2016	Sheet	90 of 94

SUSC#_PWR POWER

VGS=10V, RDson=27.6mOHM

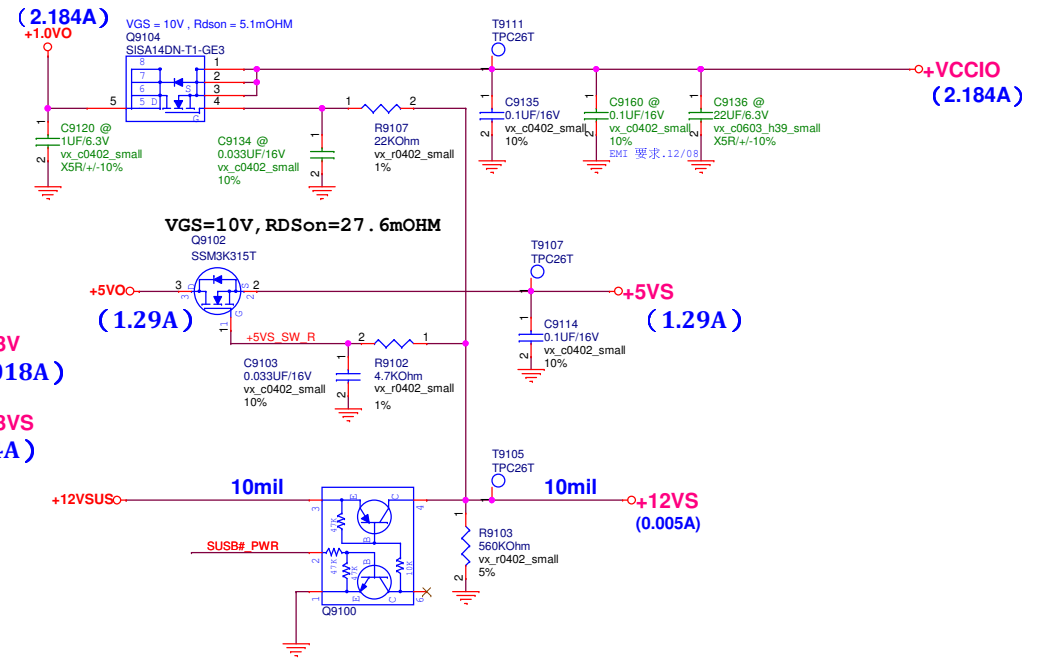


SUSC#_PWR POWER Control

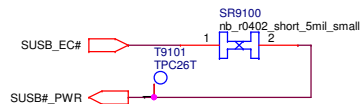


SUSB#_PWR POWER

VGS = 10V, Rds(on) = 5.1mOHM



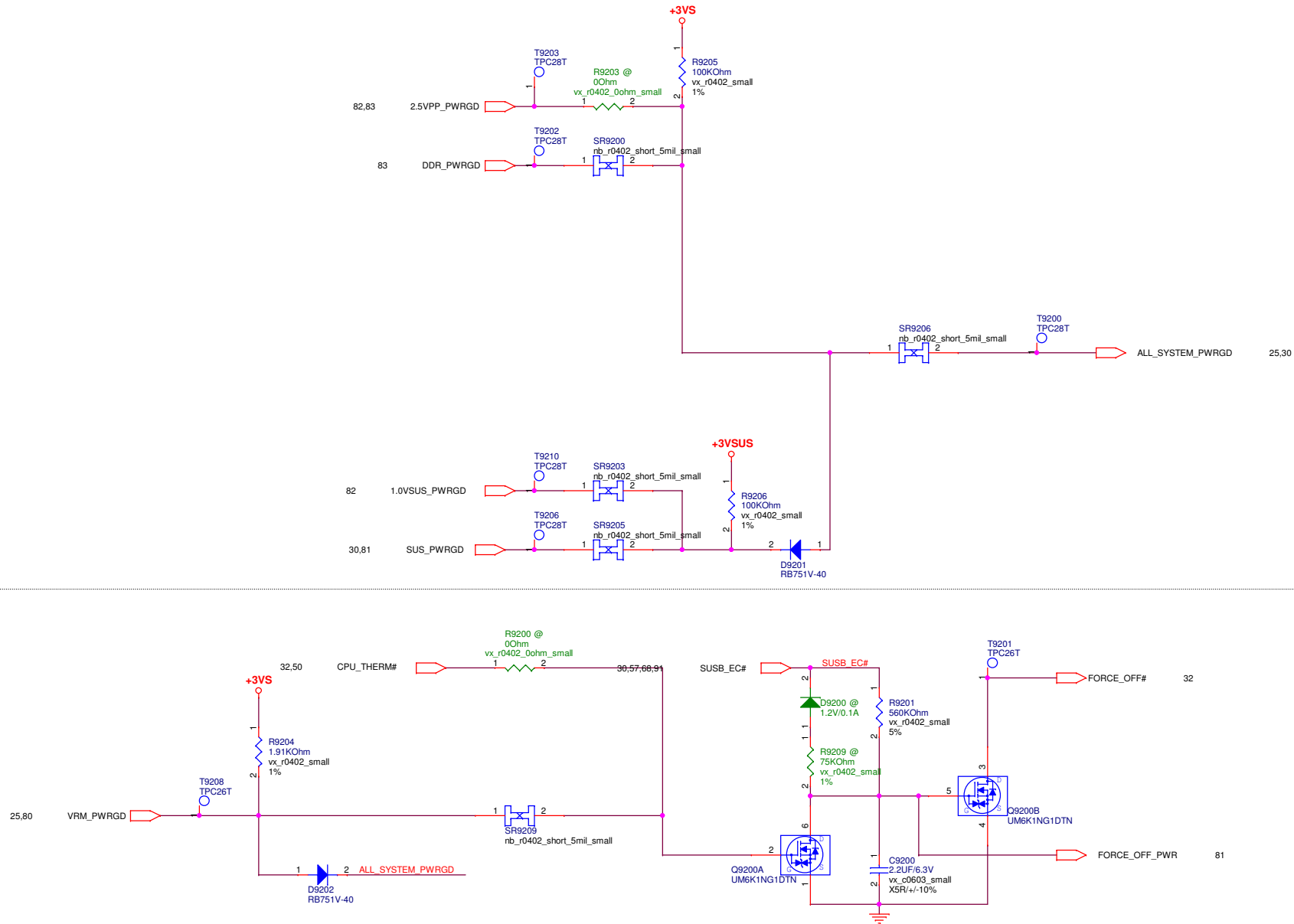
SUSB#_PWR POWER Control



<Variant Name>

PEGATRON Title : POWER_LOAD SWITCH			
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer:		Adams Lin	
Size	Project Name		Rev
Custom		X3	1.1
Date:	Wednesday, August 31, 2016	Sheet	91 of 94

POWER GOOD DETECTOR

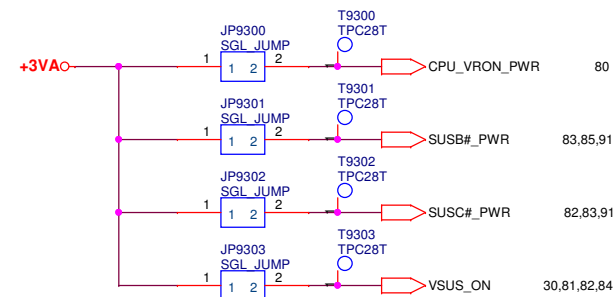


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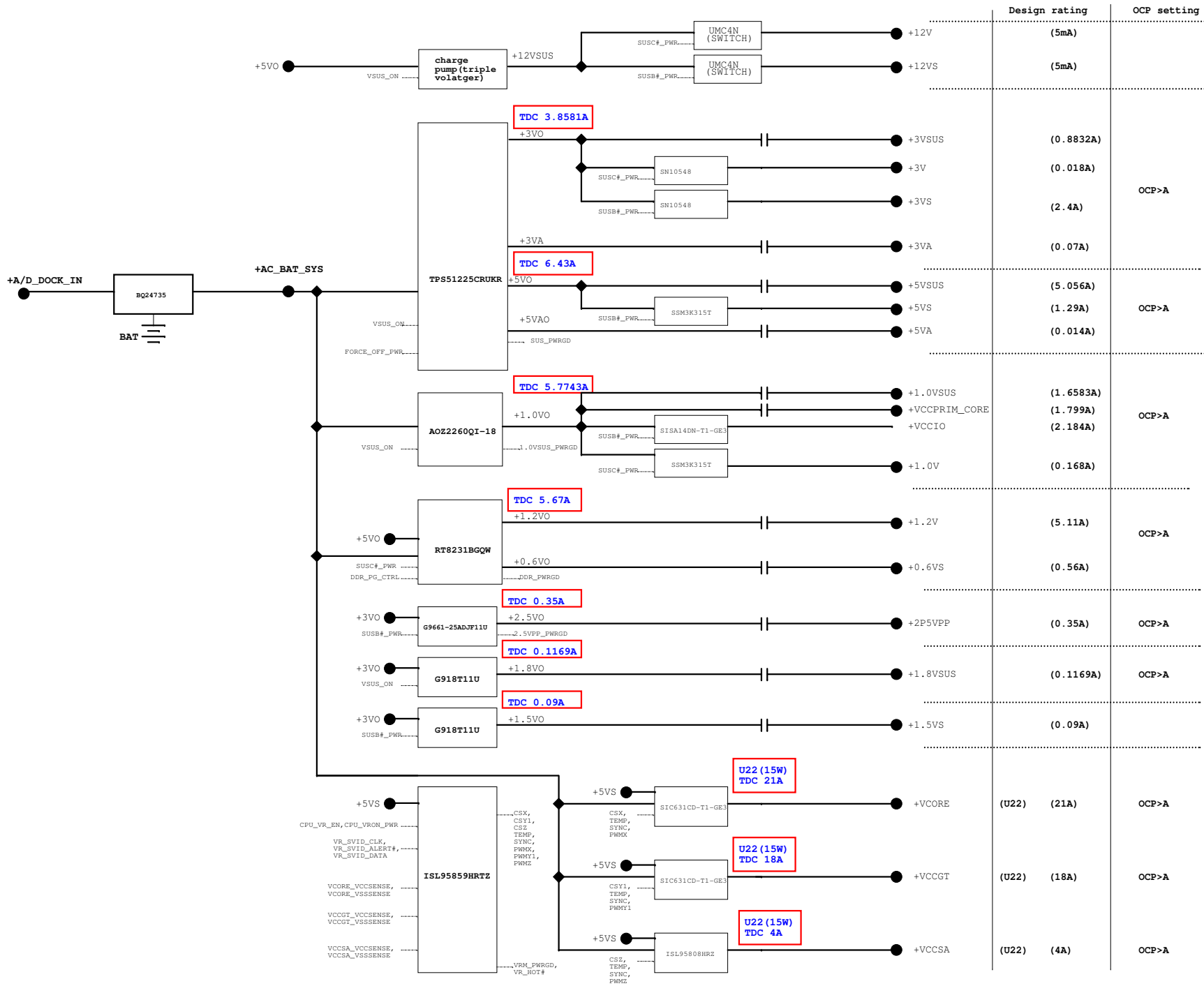
PEGATRON		Title : POWER_PROTECT	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer: Adams Lin	
Size Custom	Project Name X3	Rev 1.1	
Date:	Wednesday, August 31, 2016	Sheet	92 of 94

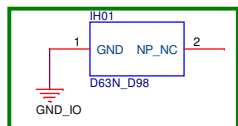
+USB_PD_IN	→	+USB_PD_IN	42,89
+A/D_DOCK_IN	→	+A/D_DOCK_IN	60,89
+AC_USBDPD_WCT_IN	→	+AC_USBDPD_WCT_IN	88,89
+AC_BAT_SYS	→	+AC_BAT_SYS	43,45,80,81,82,83,88
+BAT_CON	→	+BAT_CON	60,88
+RTC_POWER	→	+RTC_POWER	81
+5VA	→	+5VA	31,56,81
+3VA	→	+3VA	24,30,31,36,41,43,53,57,64,81,88
+5VO	→	+5VO	26,81,82,83,88,91
+3VO	→	+3VO	81,82,84,85,91
+2.5VO	→	+2.5VO	82
+1.8VO	→	+1.8VO	84
+1.2VO	→	+1.2VO	83
+1.0VO	→	+1.0VO	82,91
+0.6VO	→	+0.6VO	83
+12VSUS	→	+12VSUS	28,81,91
+5VSUS	→	+5VSUS	41,42,52,56,64,81
+3VSUS	→	+3VSUS	4,24,25,26,28,30,31,41,42,51,53,62,64,68,81,92
+1.8VSUS	→	+1.8VSUS	9,21,22,26,84
+1.0VSUS	→	+1.0VSUS	26,82
+12V	→	+12V	57,91
+2P5VPP	→	+2P5VPP	16,17,57,82
+1.2V	→	+1.2V	4,7,15,16,17,19,57,83
+1.0V	→	+1.0V	7,57,91
+12VS	→	+12VS	31,48,57,91
+5VS	→	+5VS	31,36,45,48,50,51,57,80,91
+3VS	→	+3VS	3,4,21,22,23,24,30,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92
+0.6VS	→	+0.6VS	15,57,83
+VCORE	→	+VCORE	5,80
+VCCGT	→	+VCCGT	6,80
+VCCSA	→	+VCCSA	7,80
+VCCIO	→	+VCCIO	3,7,9,57,91
+VCCPRIM_CORE	→	+VCCPRIM_CORE	26,82

FOR POWER TEST

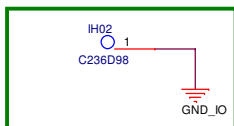


PEGATRON		Title : POWER_SIGNAL	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-POWER		Engineer: Adams Lin	
Size B	Project Name X3		Rev 1.1
Date: Wednesday, August 31, 2016		Sheet 93 of 94	

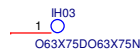




2016.6.6 R1.2_10L ---For ME

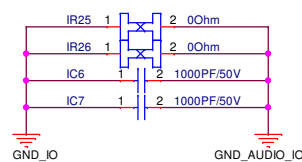
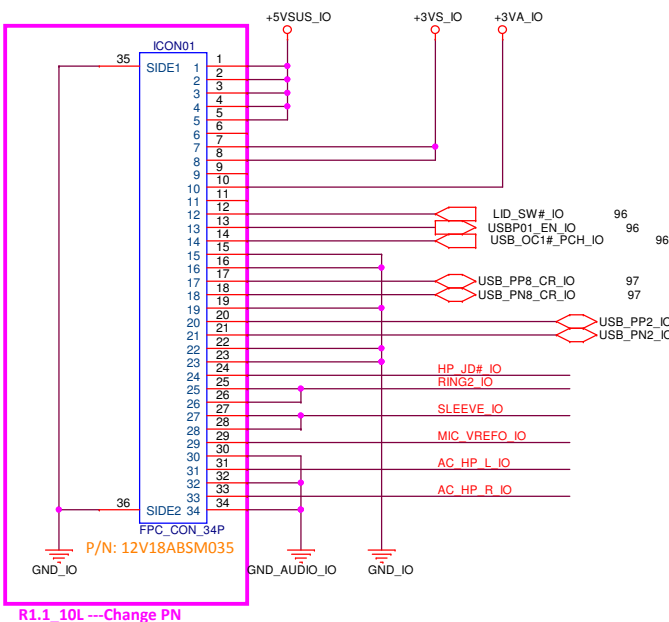
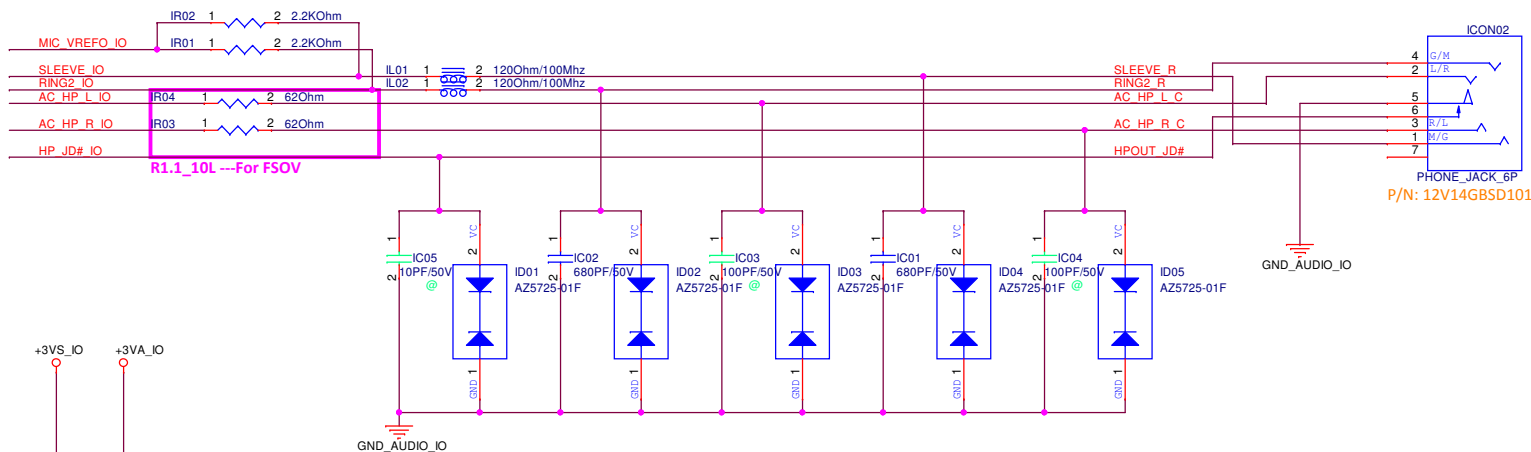


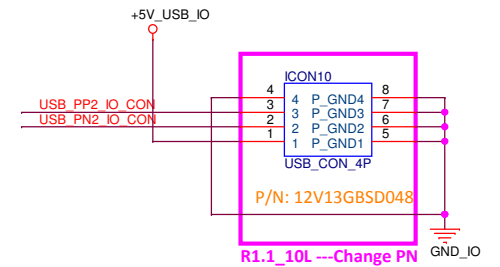
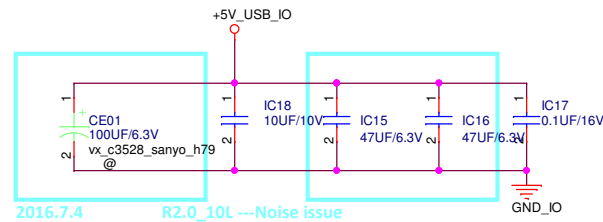
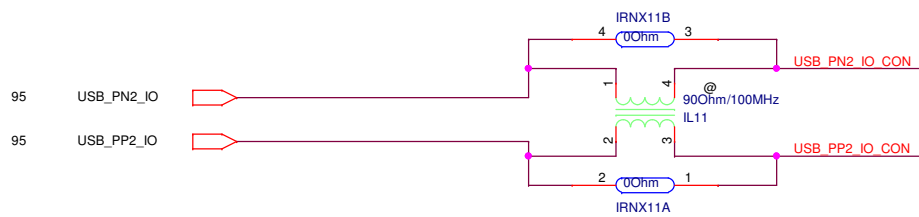
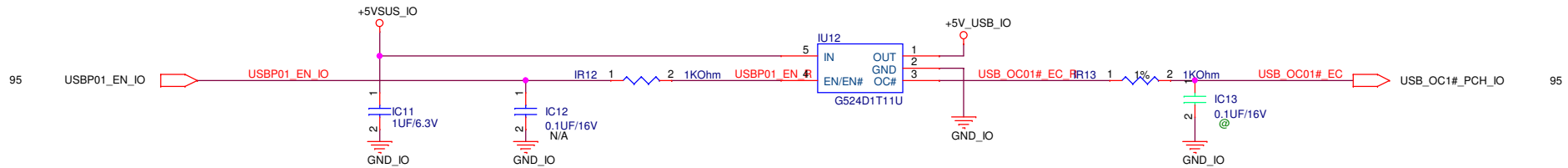
2016.6.6 R1.2_10L ---For ME



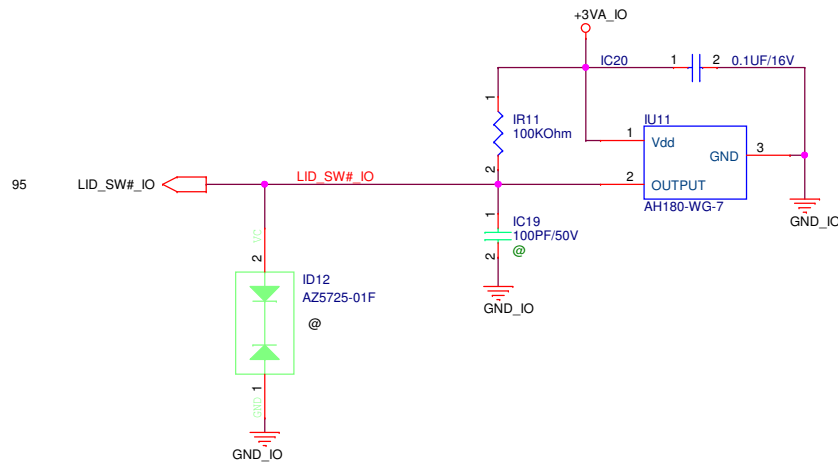
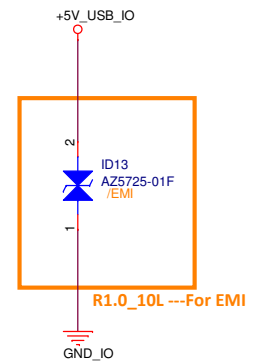
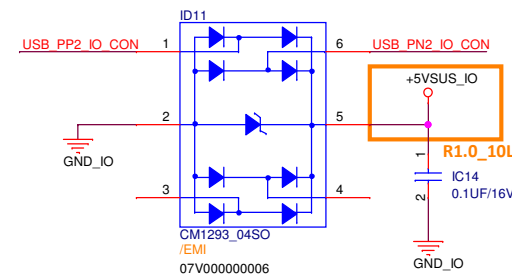
2016.7.14 R1.2_10L ---For ME

AUDIO JACK

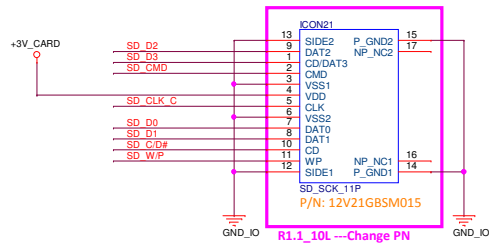
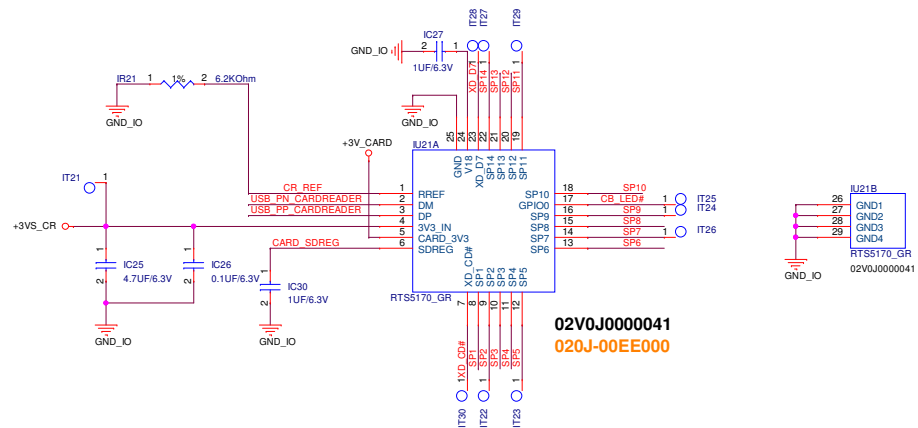
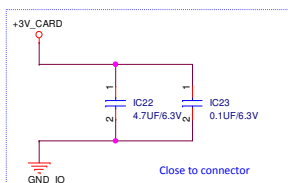
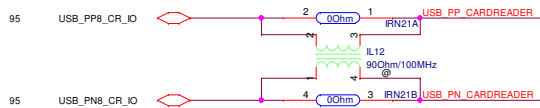
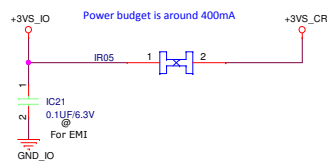




PLACE ESD Diodes near USB Connector



Cardreader



RTS5170-GR Share Pin Assignment

SP1	SD_W/P
SP3	SD_D1
SP4	SD_D0
SP6	SD_C/D#
SP8	SD_CLK
SP10	SD_CMD
SP12	SD_D3
SP13	SD_D2

<Variant Name>

PEGATRON Title : **RTS5138-GR**

Engineer: *Andy Kao*

Size	Project Name	Rev
Custom	X3	1.0

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